AiP24C64
I^2C Serial EEPROM

Product Specification

Specification Revision History ：

Version	Data	Description
2017-02-A1	2017-02-06	New-made
2024-04-B1	2024-04	Update the template

Contents

1、General Description

The AiP24C64 is a 64-Kbit I^{2}C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 8K × 8bits, which is organized in 32-byte per page.
The device is used in low-voltage and low-power systems.

Features:

- Single Supply Voltage and High Speed
  - Minimum operating voltage down to 1.7V
  - 1 MHz clock from 2.5V to 5.5V
  - 400kHz clock from 1.7V to 2.5V
- Low power CMOS technology
  - Read current 1.0mA, maximum
  - Write current 2.0mA, maximum
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- 32 byte Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - Endurance: > 1 Million Write Cycles
  - Data Retention: > 100 Years
- LATCH UP Capability: +/- 200mA
- Package: DIP8, SOP8, TSSOP8

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP24C64DA8.TB	DIP8	AiP24C64	50 PCS/tube	40 tube/box	2000 PCS/box	Dimensions of plastic enclosure: 9.2mm×6.4mm Pin spacing: 2.54mm
AiP24C64SA8.TB	SOP8	AiP24C64	100 PCS/tube	100 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
AiP24C64TB8.TB	TSSOP8	24C64	100 PCS/tube	200 tube/box	20000 PCS/box	Dimensions of plastic enclosure: 4.4mm×3.0mm Pin spacing: 0.65mm

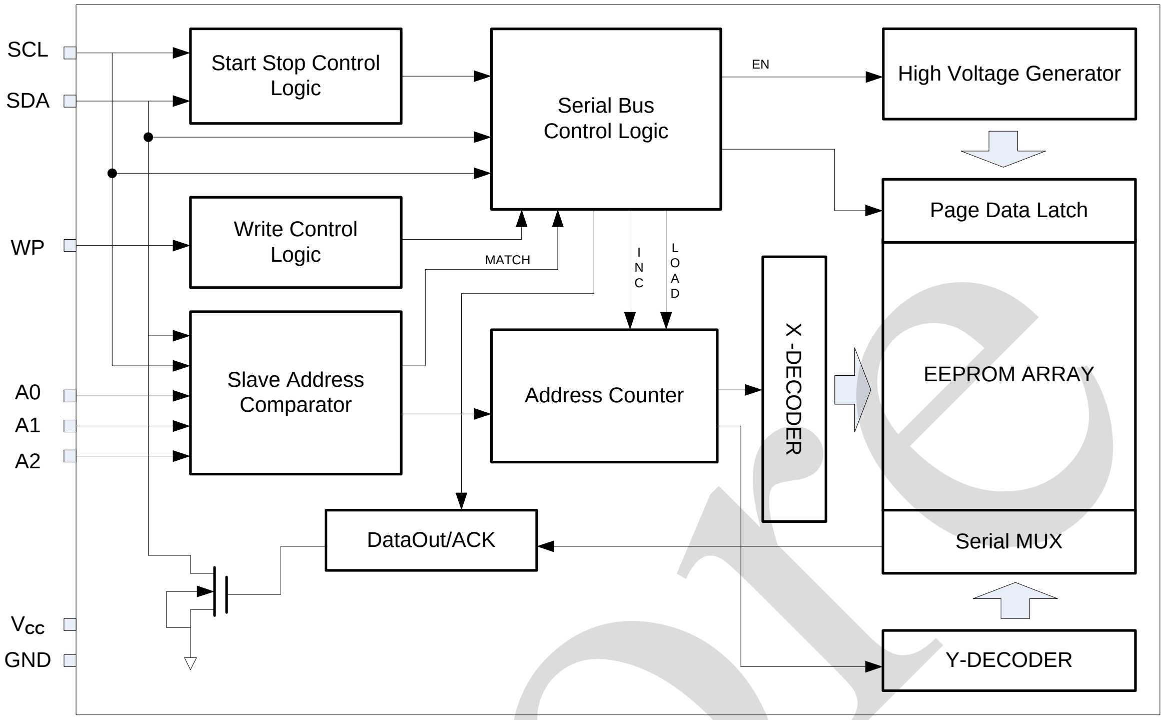
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP24C64SA8.TR	SOP8	AiP24C64	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing:1.27mm
AiP24C64TB8.TR	TSSOP8	24C64	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 4.4mm×3.0mm Pin spacing:0.65mm

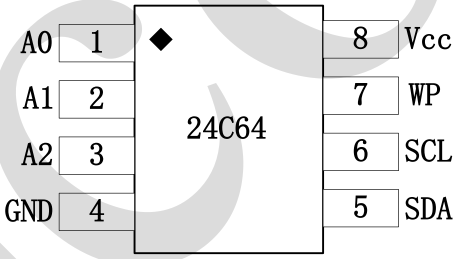
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	A0	Slave Address Setting
2	A1	Slave Address Setting
3	A2	Slave Address Setting
4	GND	Ground
5	SDA	Serial Data Input and Serial Data Output
6	SCL	Serial Clock Input
7	WP	Write Control, Low Enable Write
8	Vcc	Power

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Conditions		Value	Unit
Power Supply Voltage	Vcc	-		6.25	V
Voltage on Any Pin with Respect to Ground	V	-		-1.0 to +7.0	V
DC Output Current	I	-		5.0	mA
Input/Output Capacitance (SDA)	$C_{I/O}$	f =1.0MHz, V_{CC}=5V, $V_{I/O}$=GND		8	pF
Input Capacitance (E0,E1,E2,WP,SCL)	C_{IN}	f=1.0MHz,V_{CC}=5V, V_{IN}=GND		6	pF
Operating Temperature	T_{amb}	-		-40 to +85	℃
Storage Temperature	T_{stg}	-		-65 to +150	℃
Soldering Temperature	T_L	10s	DIP	250	℃
			SOP/TSSOP	260	

Notes:

[1] This parameter is ensured by characterization not 100% tested

[2]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2、Electrical Characteristics

3.2.1、DC Characteristics

(T_{amb}=-40℃ to +85℃, V_{CC}=+1.8V to +5.5V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	-	1.7	-	5.5	V
Standby Current	Isb	Vcc=3.3V, T_{amb}=85℃	-	-	1.0	uA
		Vcc=5.5V, T_{amb}=85℃	-	-	3.0	uA
Supply Current	I_{CC1}	Vcc=5.5V, Read at 400Khz	-	-	1.0	mA
Supply Current	I_{CC2}	Vcc=5.5V,Write at 400Khz	-	-	2.0	mA
Input Leakage Current	I_{LI}	V_{IN}=V_{CC} or GND	-	0.10	1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=V_{CC} or GND	-	0.05	1.0	µA
Input Low Level	V_{IL}	-	-0.6	-	0.3V_{CC}	V
Input High Level	V_{IH}	-	0.7V_{CC}	-	V_{CC}+0.5	V
Output Low Level	V_{OL1}	V_{CC}=1.7V (SDA) I_{OL}=1.5mA	-	-	0.2	V
Output Low Level	V_{OL2}	V_{CC}=3.0V (SDA) I_{OL}=2.1mA	-	-	0.4	V

Notes: [1] This parameter is ensured by characterization not 100% tested

3.2.2、AC Characteristics

(Unless otherwise specified, V_{CC}=1.8V to 5.5V, T_{amb}=-40℃ to +85℃, C_L=100pF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Frequency, SCL	fSCL	V_{CC}=1.7V	-	-	400	kHz
		V_{CC}=2.7V	-	-	1000	
		V_{CC}=5.0V	-	-	1000	
Clock Pulse Width Low	tLOW	V_{CC}=1.7V	1.3	-	-	us
		V_{CC}=2.7V	0.4	-	-	
		V_{CC}=5.0V	0.4	-	-	
Clock Pulse Width High	t_{HIGH}	V_{CC}=1.7V	0.6	-	-	us
		V_{CC}=2.7V	0.4	-	-	
		V_{CC}=5.0V	0.4	-	-	
Noise Suppression Time	t_I	V_{CC}=1.7V	-	-	100	ns
		V_{CC}=2.7V	-	-	50	
		V_{CC}=5.0V	-	-	50	
Clock Low to Data Out Valid	t_{AA}	V_{CC}=1.7V	0.05	-	0.9	us
		V_{CC}=2.7V	0.05	-	0.55	
		V_{CC}=5.0V	0.05	-	0.55	
Time the bus must be free before a new transmission can start	t_{BUF}	V_{CC}=1.7V	1.3	-	-	us
		V_{CC}=2.7V	0.5	-	-	
		V_{CC}=5.0V	0.5	-	-	
Start Hold Time	$t_{HD.STA}$	V_{CC}=1.7V	0.6	-	-	us
		V_{CC}=2.7V	0.25	-	-	
		V_{CC}=5.0V	0.25	-	-	
Start Setup Time	$t_{SU.STA}$	V_{CC}=1.7V	0.6	-	-	us
		V_{CC}=2.7V	0.25	-	-	
		V_{CC}=5.0V	0.25	-	-	
Data In Hold Time	$t_{HD.D}$	V_{CC}=1.7V	0	-	-	us
		V_{CC}=2.7V	0	-	-	
		V_{CC}=5.0V	0	-	-	
Data In Setup Time	$t_{SU.D}$	V_{CC}=1.7V	100	-	-	ns
		V_{CC}=2.7V	100	-	-	
		V_{CC}=5.0V	100	-	-	
Inputs Rise Time[1]	t_R	V_{CC}=1.7V	-	-	300	ns
		V_{CC}=2.7V	-	-	300	
		V_{CC}=5.0V	-	-	300	
Inputs Fall Time[1]	t_F	V_{CC}=1.7V	-	-	300	ns
		V_{CC}=2.7V	-	-	300	
		V_{CC}=5.0V	-	-	100	
Stop Setup Time	$t_{SU.STO}$	V_{CC}=1.7V	0.6	-	-	us
		V_{CC}=2.7V	0.25	-	-	
		V_{CC}=5.0V	0.25	-	-	
Data Out Hold Time	t_{DH}	V_{CC}=1.7V	50	-	-	ns
		V_{CC}=2.7V	50	-	-	
		V_{CC}=5.0V	50	-	-	
WP pin Setup Time	$t_{SU.WP}$	V_{CC}=1.7V	1.2	-	-	us

		V_{CC}=2.7V	0.6	-	-	
		V_{CC}=5.0V	0.6	-	-	
WP pin Hold Time	$t_{HD.WP}$	V_{CC}=1.7V	1.2	-	-	us
		V_{CC}=2.7V	0.6	-	-	
		V_{CC}=5.0V	0.6	-	-	
Write Cycle Time	t_{WR}	V_{CC}=1.7V	-	-	5	ms
		V_{CC}=2.7V	-	-	5	
		V_{CC}=5.0V	-	-	5	
Endurance	EDR	3.3V, Page mode	1,000,000	-	-	Write cycles
Data retention	DRET	-	100	-	-	Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

4、Function Description

4.1、Device Operation

4.1.1、Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

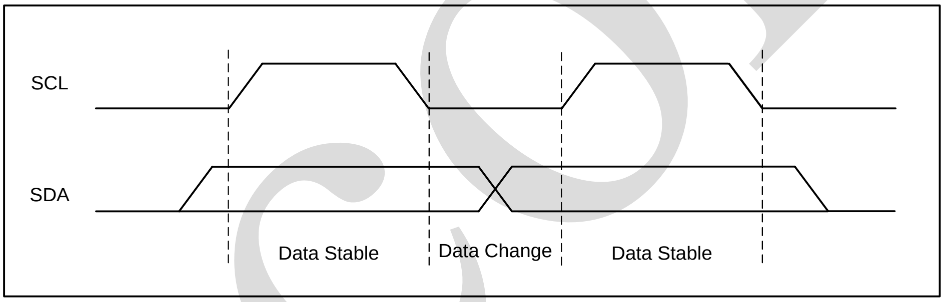


Figure 4-1

4.1.2、Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

4.1.3、Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the AiP24C64 in a standby power mode (see Figure 4-2)

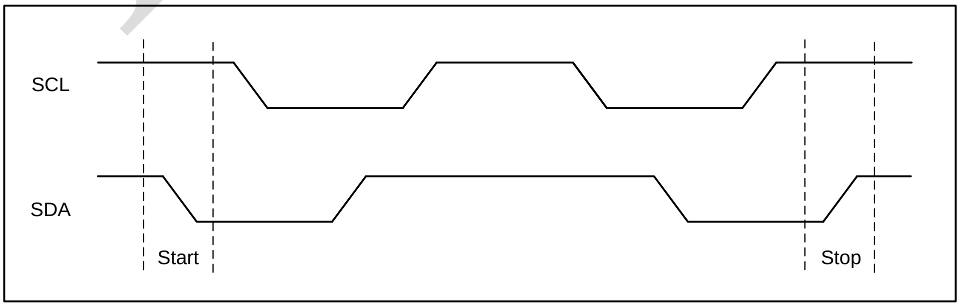


Figure 4-2

4.1.4、Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the AiP24C64 in 8-bit words. The AiP24C64 sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle(see to Figure 4-3).

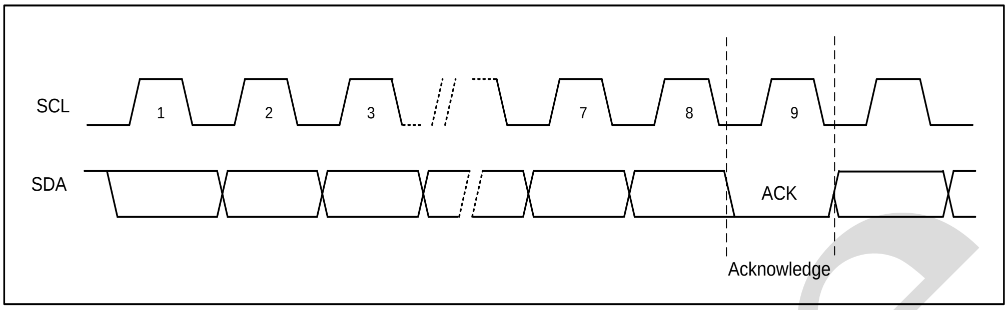


Figure 4-3

4.1.5、Standby Mode

The AiP24C64 features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation.

4.1.6、Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed(see to Figure 4-4).

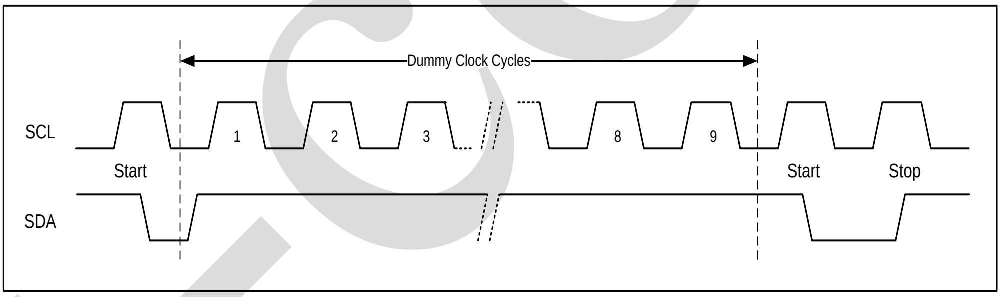


Figure 4-4

4.1.7、Bus Timing(see to Figure 4-5)

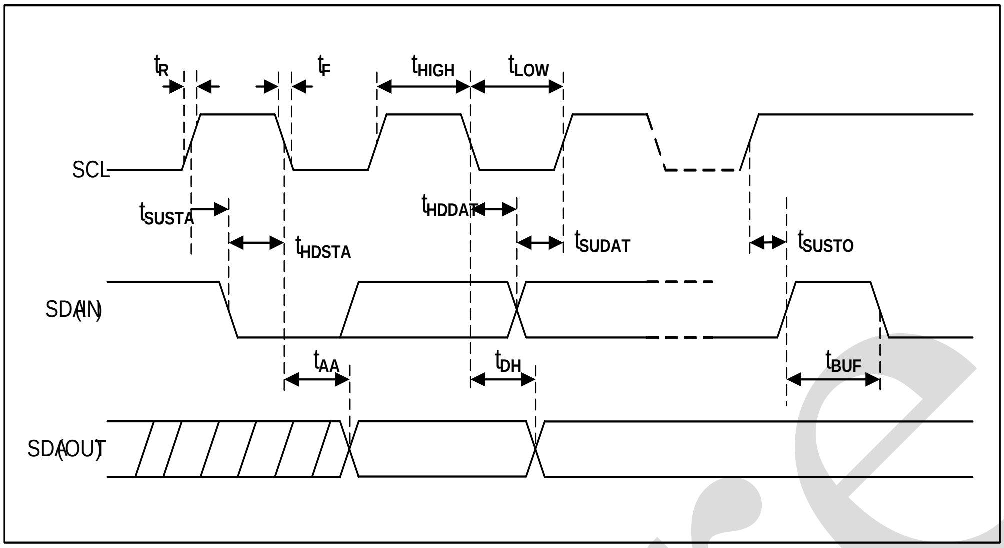


Figure 4-5

4.1.8、Write Cycle Timing(see to Figure 4-6)

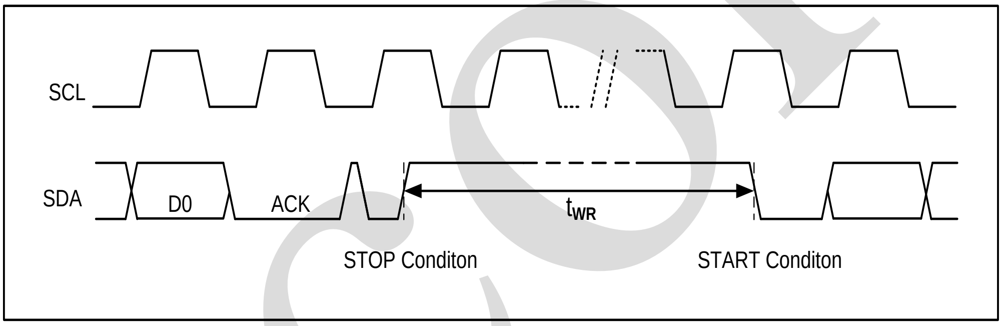


Figure 4-6

4.2、Device Addressing

The AiP24C64 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table below). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

Table 4-1 Device Address

Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	1	0	1	0	A2	A1	A0	R/W

Table 4-2 First Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	X	X	X	B12	B11	B10	B9	B8

Table 4-3 Second Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	B7	B6	B5	B4	B3	B2	B1	B0

The three A2, A1, and A0 device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

4.3、Data Security

AiP24C64 has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at Vcc.

4.4、Write Operations

4.4.1、Byte Write

A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the AiP24C64 will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the AiP24C64 will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the AiP24C64 enters an internally timed write cycle, all inputs are disabled during this write cycle and the AiP24C64 will not respond until the write is complete (see Figure 4-7).

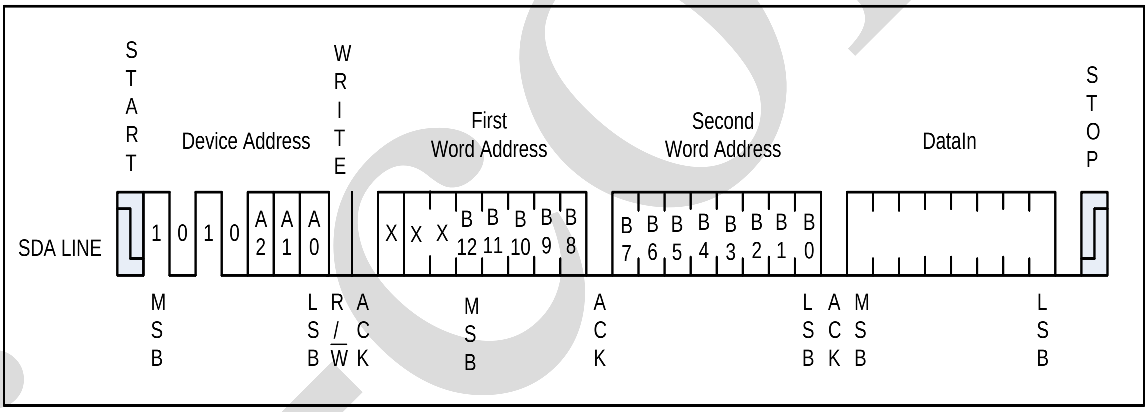
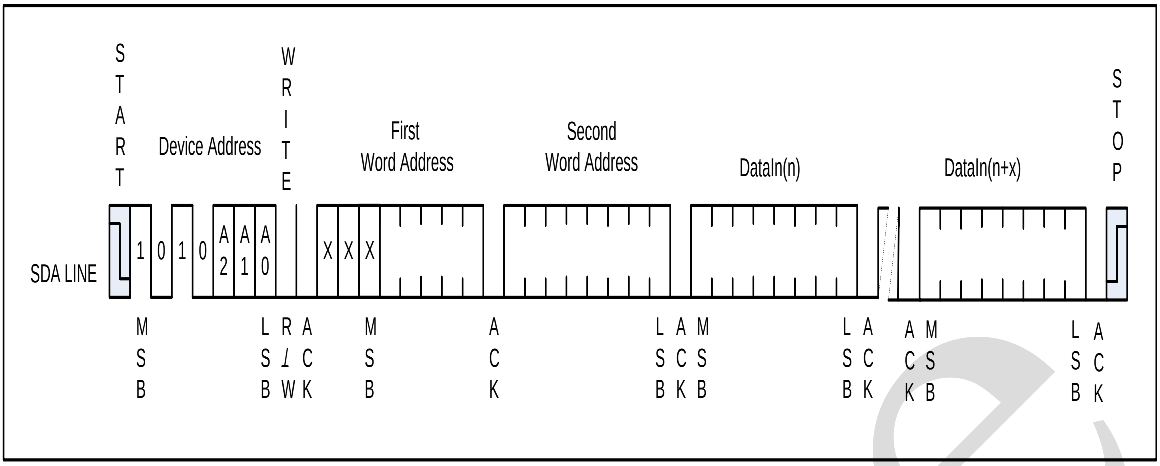


Figure 4-7

Notes: [1] x means don’t care bits.

4.4.2、Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the AiP24C64 acknowledges receipt of the first data word, the master can transmit more data words. The AiP24C64 will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition. (see Figure 4-8).



see Figure 4-8

Notes: [1] x means don't care bits.

The lower five bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the AiP24C64, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

4.4.3、Acknowledge Polling

Once the internally timed write cycle has started and the AiP24C64 inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the AiP24C64 respond with a "0", allowing the read or write sequence to continue.

4.5、Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: Current Address Read; Random Address Read and Sequential Read.

4.5.1、Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the AiP24C64, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 4-9).

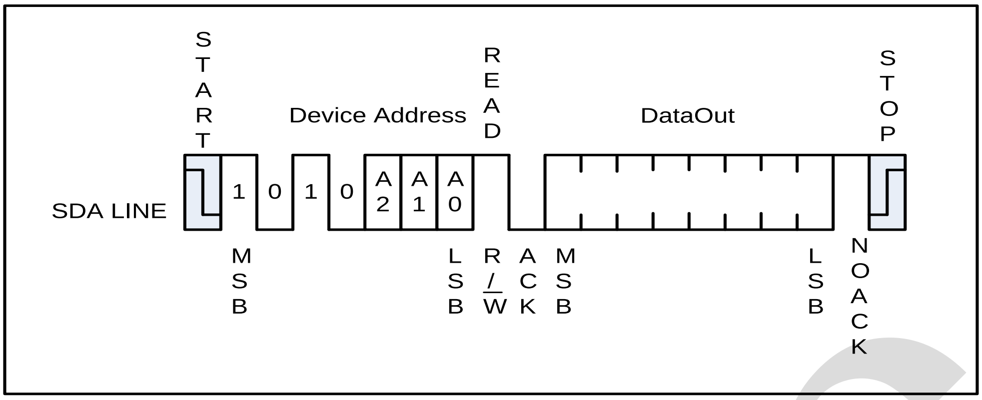


Figure 4-9

4.5.2、Random Read

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the AiP24C64, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The AiP24C64 acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 4-10).

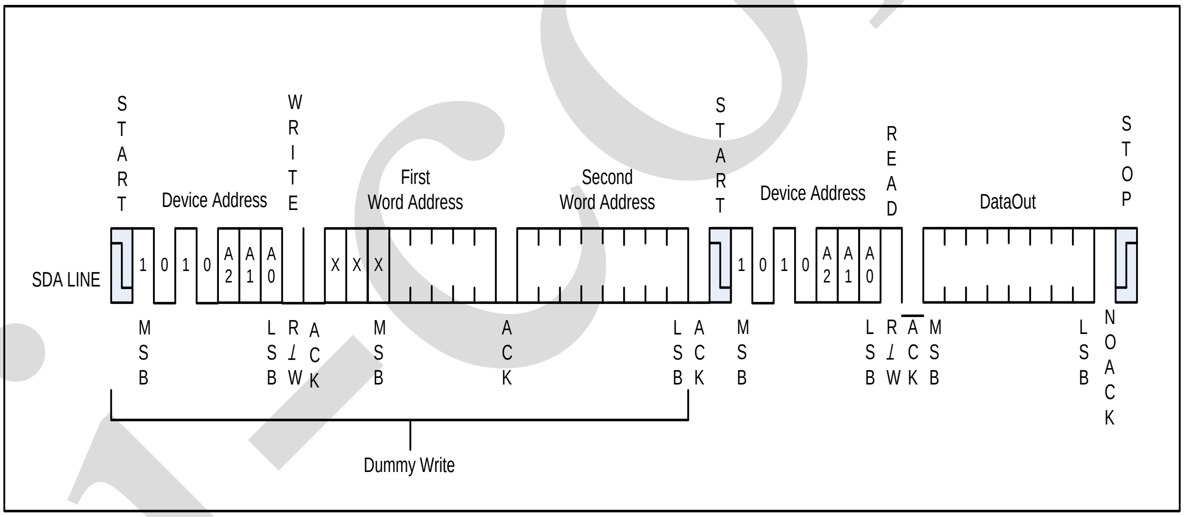


Figure 4-10

Notes: [1] x means don’t care bits.

4.5.3、Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the AiP24C64receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 4-11)

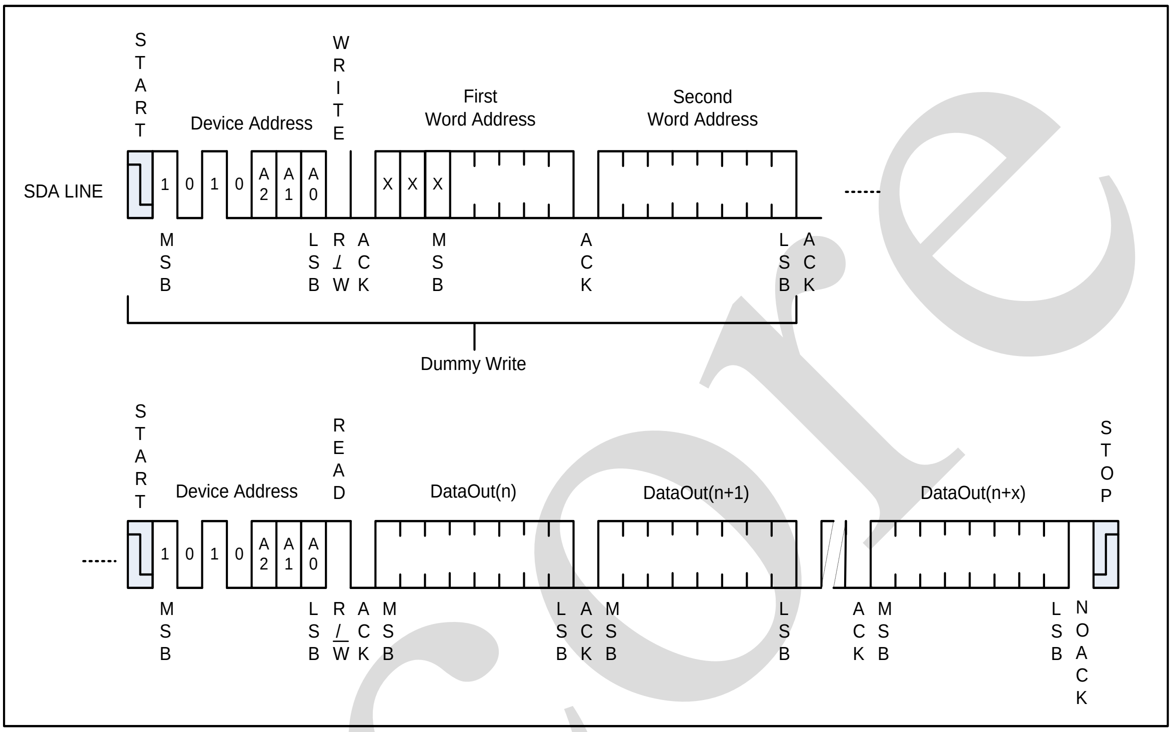
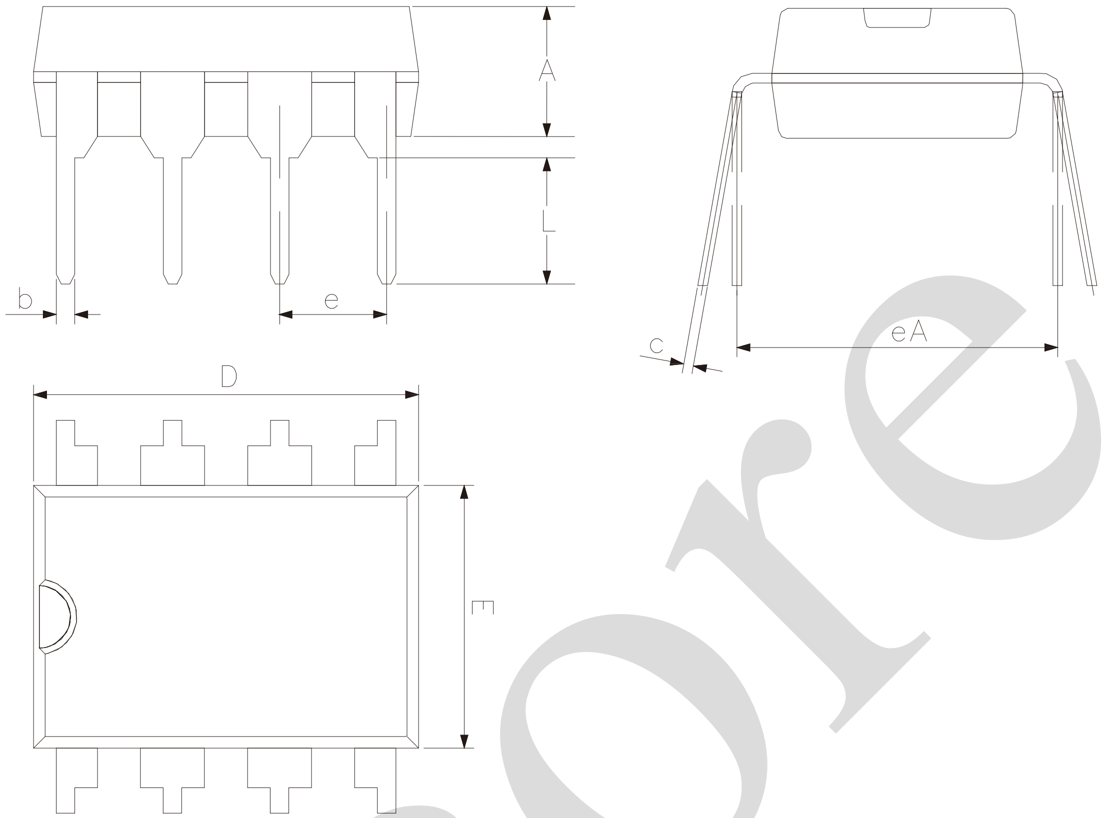


Figure 4-11

Notes: [1] x means don’t care bits.

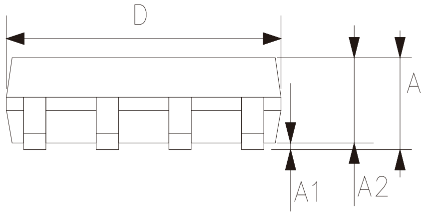
5、Package Information

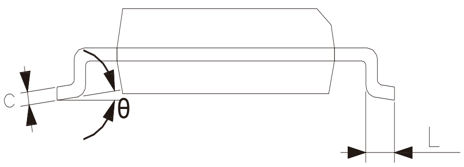
5.1、DIP8

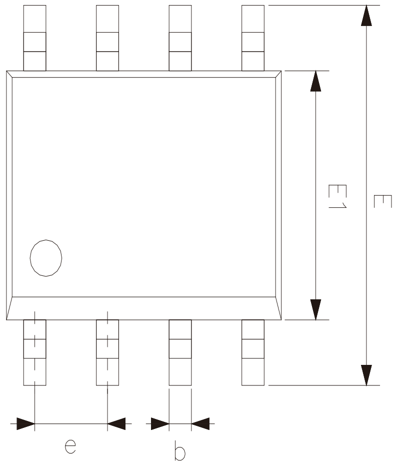


2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	3.00	3.60
b	0.36	0.56
c	0.20	0.36
D	9.00	9.45
E	6.15	6.60
e	2.54	
eA	7.62	9.30
L	3.00	—

5.2、SOP8

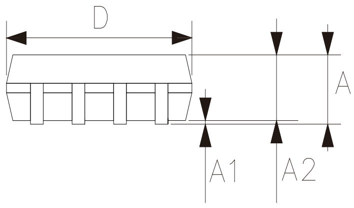


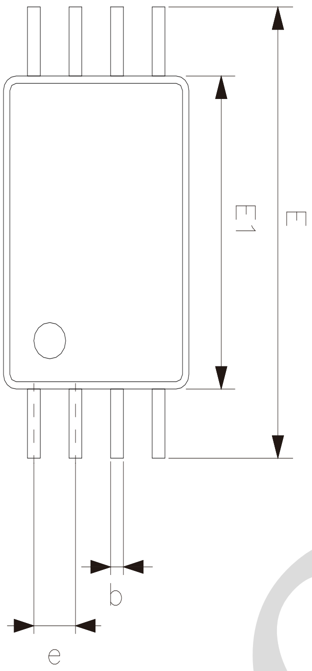




2023/12/A	Dimensions In Millimeters	
Symbol	**Min.**	**Max.**
A	1.35	1.80
A1	0.05	0.25
A2	1.25	1.55
D	4.70	5.10
E	5.80	6.30
E1	3.70	4.10
b	0.306	0.51
c	0.19	0.25
e	1.27	
L	0.40	0.89
θ	0°	8°

5.3、TSSOP8





2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests i-Core's application to avoid failure in the application or the application of the customer' s third party users. I-Core does not accept any liability.

The Company reserves the right to change or improve the information published in this chapter at any time. The information in this chapter are subject to change without notice. We recommend the customer to consult our sales staff before purchasing.

Please obtain related materials form i-Core's regular channels and we are not responsible for its content if it is provided by sources other than our company.

In case of any conflict between the Chinese and English version, the version is subject to the Chinese one.