AiP1302
Trickle-Charge Timekeeping Chip

Product Specification

Specification Revision History：

Version	Date	Description
2015-12-A1	2015-12	New
2018-07-A2	2018-07	Replace the template; add ordering information
2022-01-A3	2022-01	Modify the ordering information
2022-11-B1	2022-11	Replace the template
2025-01-B2	2025-01	Add the package form for DFN8

Contents

1、General Description

AiP1302 is a trickle charge clock chip circuit, which includes clock/calendar register and 31-byte data temporary register. The real-time clock/calendar provides information including seconds, minutes, hours, dates, months and years. Leap year can be adjusted by itself. You can choose 12-hour system and 24-hour system, and you can set AM and PM. Data transmission is controlled through three wires: CE, I/O and SCLK.

Features:

- Clock counting function, leap year adjustment valid up to 2100.
- 3-wire transmission
- Built-in 31-byte RAM register
- Operating voltage: 2.0 to 5.5V
- Operating current is less than 400nA (V_{CC2}=2.0V)
- TTL compatible
- Battery or super capacitor (more than 0.1F) can be used for backup power supply.
- Package form: SOP8/DIP8/TSSOP8/DFN8

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP1302SA8.TB	SOP8	AiP1302	100 PCS/tube	100 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
AiP1302DA8.TB	DIP8	AiP1302	50 PCS/tube	40 tube/box	2000 PCS/box	Dimensions of plastic enclosure: 9.2mm×6.4mm Pin spacing: 2.54mm
AiP1302TB8.TB	TSSOP8	BT	100 PCS/tube	200 tube/box	20000 PCS/box	Dimensions of plastic enclosure: 3.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP1302SA8.TR	SOP8	AiP1302	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
AiP1302TB8.TR	TSSOP8	BT	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 3.0mm×4.4mm Pin spacing: 0.65mm
AiP1302XF8.TR	DFN8	AiP1302	3000PCS/reel	30000PCS/box	Dimensions of plastic enclosure: 3.0mm×2.0mm Pin spacing: 0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

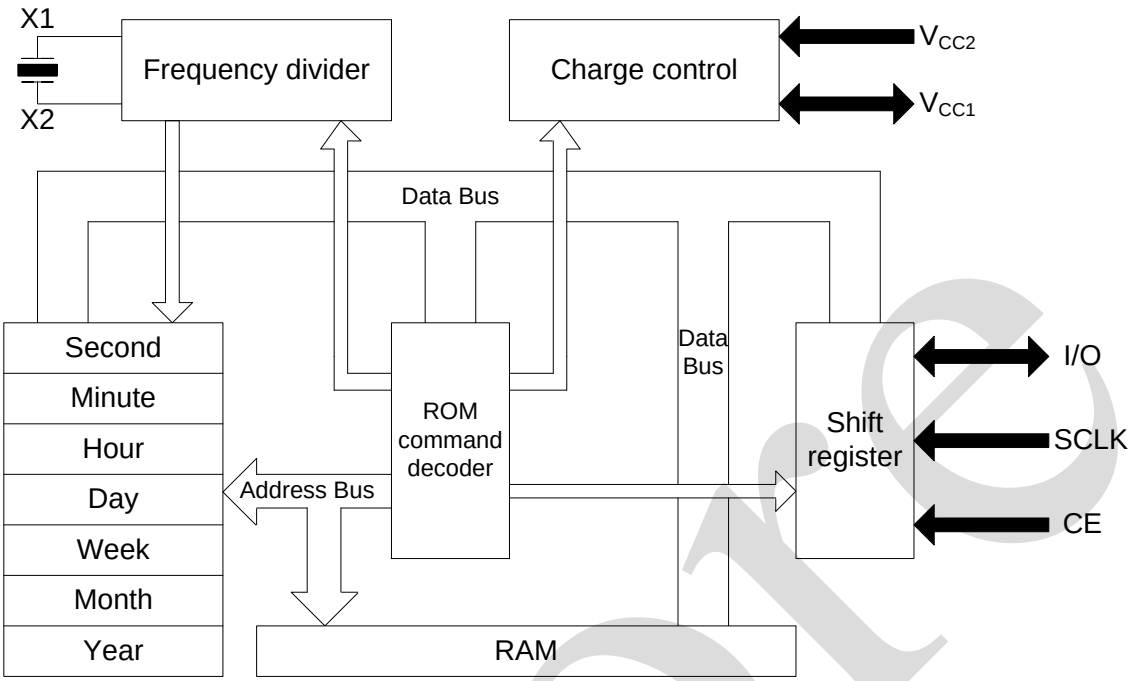
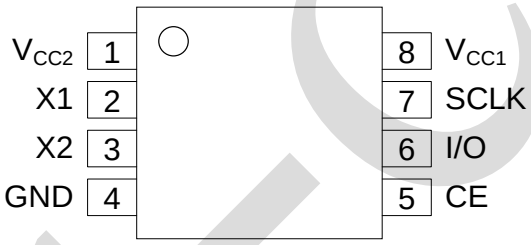
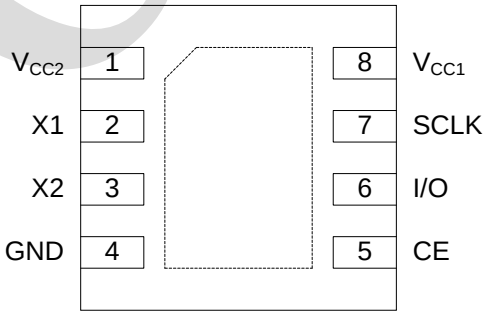


Figure 1. Block Diagram

2.2、Pin Configuration



DIP8/SOP8/TSSOP8



DFN8

2.3、Pin Description

Pin	Symbol	Function
1	V_{CC2}	Dual power supply- primary power supply, Vcc2 will supply the power when V_{CC2}>V_{CC1}+0.2V
2	X1	32.768KHz crystal pin
3	X2	32.768KHz crystal pin
4	GND	Ground
5	CE	Chip selection signal
6	I/O	Data input/output port
7	SCLK	Serial clock input
8	V_{CC1}	Dual power supply- backup power supply,V_{CC1} will supply the power when V_{CC2}<V_{CC1}+0.2V

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to Vss, unless otherwise specified)

Characteristic	Symbol	Conditions		Value	Unit
Power Supply Voltage	V_{CC1}, V_{CC2}	-		2.0~5.5	V
High-Level Input Voltage	V_{IH}	-		V_{CC}+0.3	V
Low-Level Input Voltage	V_{IL}	V_{CC}=2.0V		0.3	V
		V_{CC}=5.0V		0.8	
Operating Temperature	T_{amb}	-		-40~85	℃
Storage Temperature	T_{stg}	-		-65~150	℃
Soldering Temperature	T_L	10s	DIP	250	℃
			SOP/TSSOP/DFN	260	

3.2、Electrical Characteristics

3.2.1、DC Characteristics

(T_{amb}=25℃, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{CC1} Operating Current	I_{CC1A}	V_{CC1}=2.0V, V_{CC2}=0V, I/O is suspended, CE is high, and crystal is enabled	-	-	0.4	mA
		V_{CC1}=5.0V, V_{CC2}=0V, I/O is suspended, CE is high, and crystal is enabled	-	-	1.2	mA
V_{CC1} Timekeeping Current	I_{CC1T}	V_{CC1}=2.0V, V_{CC2}=0V, I/O is suspended, CE and SCLK are low, and crystal is enabled	-	0.2	1	uA
		V_{CC1}=5.0V, V_{CC2}=0V, I/O is suspended, CE and SCLK are low, and crystal is enabled	-	0.45	2	uA
V_{CC1} Quiescent Current	I_{CC1S}	V_{CC1}=2.0V, V_{CC2}=0V, CE, I/O, SCLK are suspended, turn off the crystal	-	0.2	1	uA
		V_{CC1}=5.0V, V_{CC2}=0V, CE, I/O, SCLK are suspended, turn off the crystal	-	0.45	2	uA
V_{CC2} Operating Current	I_{CC2A}	V_{CC2}=2.0V, V_{CC1}=0V, I/O is suspended, CE is high, and crystal is enabled	-	-	0.4	mA
		V_{CC2}=5.0V, V_{CC1}=0V, I/O is suspended, CE is high, and crystal is enabled	-	-	1.3	mA
V_{CC2} Timekeeping Current	I_{CC2T}	V_{CC2}=2.0V, V_{CC1}=0V，I/O is suspended, CE and SCLK are low, and crystal is enabled	-	-	25	uA
		V_{CC2}=5.0V, V_{CC1}=0V, I/O is suspended, CE and SCLK are low, and crystal is enabled	-	-	81	uA

V_{CC2} Quiescent Current	I_{CC2S}	V_{CC2}=2.0V, V_{CC1}=0V, CE, I/O, SCLK are suspended, turn off the crystal	-	-	25	uA
		V_{CC2}=5.0V, V_{CC1}=0V, CE, I/O, SCLK are suspended, turn off the crystal	-	-	80	uA
Input Leakage Current	I_{Ll}	CE, I/O, SCLK	-	85	500	uA
Output High-Level Voltage	V_{OH}	V_{CC}=2.0V, I_{OH}=-1mA	1.6	-	-	V
		V_{CC}=5.0V, I_{OH}=-0.4mA	2.4	-	-	V
Output Low-Level Voltage	V_{OL}	V_{CC}=2.0, I_{OL}=4mA	-	-	0.4	V
		V_{CC}=5.0V, I_{OL}=1.5mA	-	-	0.4	V
Trickle Charge Resistor	R1	-	-	2	-	KΩ
	R2	-	-	4	-	KΩ
	R3	-	-	8	-	KΩ
Trickle Charge Diode Voltage Drop	V_{TD}	-	-	0.7	-	V

3.2.2、AC Characteristics

(T_{amb}=25℃, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Establishment	T_{dc}	V_{CC}=2.0V, Note 1	200	-	-	ns
		V_{CC}=5.0V, Note 1	50	-	-	ns
Data Hold	T_{cdh}	V_{CC}=2.0V, Note 1	280	-	-	ns
		V_{CC}=5.0V, Note 1	70	-	-	ns
Data Delay	T_{cdd}	V_{CC}=2.0V, CL=50pF, Note 1, 2	-	-	800	ns
		V_{CC}=5.0V, CL=50pF, Note 1, 2	-	-	200	ns
Clock Low-Level	T_{cl}	V_{CC}=2.0V, Note 1	1000	-	-	ns
		V_{CC}=5.0V, Note 1	250	-	-	ns
Clock High-Level	T_{ch}	V_{CC}=2.0V, Note 1	1000	-	-	ns
		V_{CC}=5.0V, Note 1	250	-	-	ns
Clock Frequency	T_{clk}	V_{CC}=2.0V, Note 1	-	-	0.5	MHz
		V_{CC}=5.0V, Note 1	-	-	2.0	MHz
Clock Rising /Falling Edge	T_r、T_f	V_{CC}=2.0V, Note 1	-	-	2000	ns
		V_{CC}=5.0V, Note 1	-	-	500	ns
CE Establishment	T_{CC}	V_{CC}=2.0V, Note 1	4	-	-	us
		V_{CC}=5.0V, Note 1	1	-	-	us
CE Hold	T_{cch}	V_{CC}=2.0V, Note 1	240	-	-	ns
		V_{CC}=5.0V, Note 1	60	-	-	ns
CE Invalid	T_{cwh}	V_{CC}=2.0V, Note 1	4	-	-	us
		V_{CC}=5.0V, Note 1	1	-	-	us
CE to IO end	T_{cdz}	V_{CC}=2.0V, Note 1	-	-	280	ns
		V_{CC}=5.0V, Note 1	-	-	70	ns
Clock to IO end	T_{ccz}	V_{CC}=2.0V, Note 1	-	-	280	ns
		V_{CC}=5.0V, Note 1	-	-	70	ns

1. Test condition is: V_{IH}=2V or V_{IL}=0.8V, and the rising edge and the falling edge are 10ns at most.
2. Test condition is: V_{IH}=2.4V or V_{IL}=0.4V, and the rising edge and the falling edge are 10ns at most.

4、Test Circuit

4.1、Data Propagation—Read

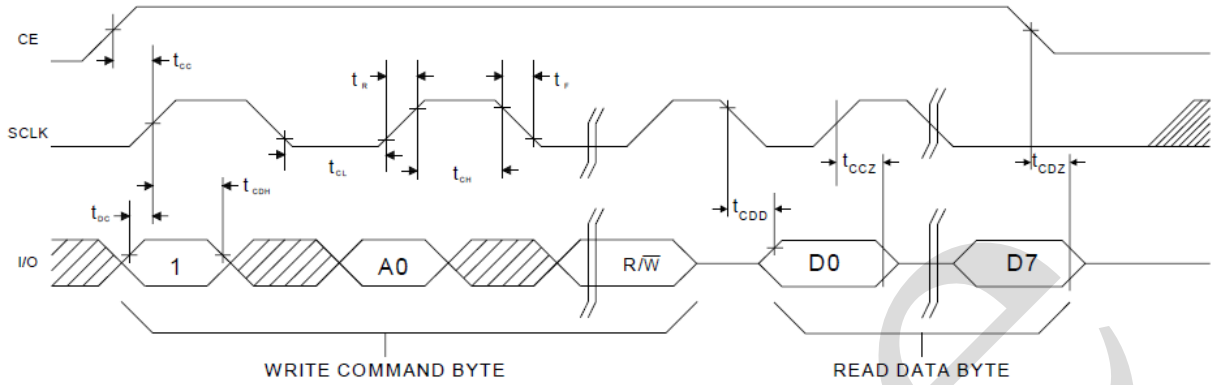


Figure 4. Data Propagation

4.2、Data Propagation—Write

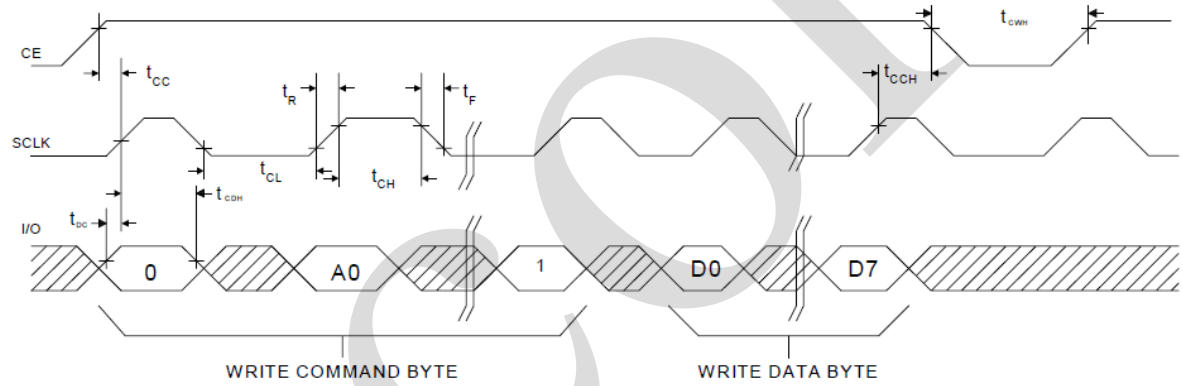


Figure 5. Data Propagation

5、Function Description

5.1、Crystal Type Selection

AiP1302 is attached with 32.768KHz crystal. Several parameters of external crystals are as follows:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Center Frequency	fo	-	32.768	-	KHz
Resonant Resistance	ESR	-	-	45	KΩ
Load Capacitor	C_L	-	12.5	-	pF

5.2、Control Instruction

Control instruction is shown as follows. Each data propagation is initiated by specified by the control instruction. The highest bit——Bit7 of the control instruction must be “1”. If it is “0”, writing is prohibited. If Bit 6 is “0”, it specifies that the clock/calendar register is controlled to read and write. While if it is “1”, it indicates that the RAM area data is controlled to read and write. Bit 1 to Bit 5 indicate register reading and writing addresses. The lowest one is Bit 0 and its value indicates input or output, “0” indicates input and “1” indicates output.

7	6	5	4	3	2	1	0
1	RAM $\overline{CK}$	A4	A3	A2	A1	A0	RD $\overline{WR}$

Figure 6. Control Instruction

5.3、Reset and Clock Control

When CE is at high level, addresses/commands are allowed to be transmitted into the shift register. In data propagation, the rising edge of the clock data must be valid, while the data bits are output at the falling edge of the clock. If CE is set to low level during the propagation, the data propagation will be terminated and the I/O pin will become high impedance state. During power-on operation, CE must remain low until VCC>2.5V. Only when SCLK is low can CE be set to high level. I/O is the serial data input and output port, and SCLK is the input port.

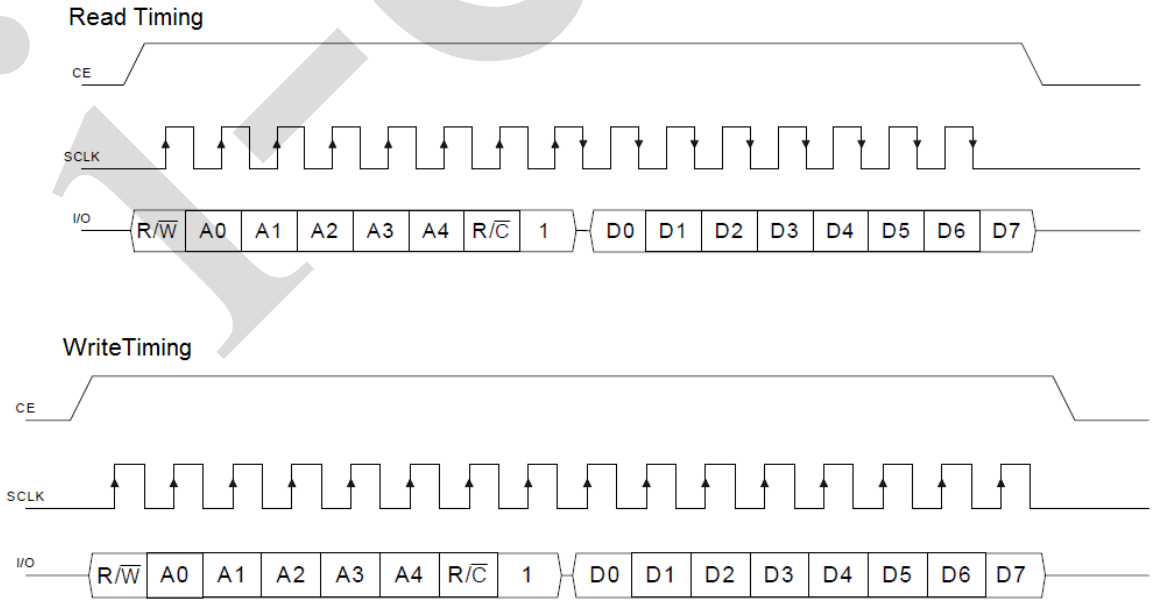


Figure 7.Read and Write Timing

5.3.1、Data Input

After 8 clock cycles, the control instruction is configured as input, and the input of one byte will be completed on the rising edge of the next 8 clock cycles, and the data propagation starts from the lowest bit of the byte.

5.3.2、Data Output

After 8 SCLK cycles of the write command byte, the data is output along the falling edge of subsequent 8 SCLK cycles. Output begins at the falling edge of the clock where the last bit of control instruction is located, and CE is required to remain high level.

5.4、Power-On Reset

The main function of power-on reset module is to reset all the time registers and control register groups during the power-on process and set an initial state like “Monday, 2000.01.01–00: 00: 00”.

5.5、Clock/Calendar

The clock/calendar contains seven registers, shown as follows. The data in the clock/calendar register is in binary coded decimal format (BCD code).

Read	Write	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BT1	BIT0	范围
81h	80h	CH	10 Seconds			Seconds				00-59
83h	82h	0	10 Minutes			Minutes				00-59
85h	84h	12/24	0	10 AM/PM	Hour	Hours				1-12/0-23
87h	86h	0	0	10Days		Day				1-31
89h	88h	0	0	0	10 月	Month				1-12
8Bh	8Ah	0	0	0	0	0	Week			1-7
8Dh	8Ch	10 Year				Year				00-99
8Fh	8Eh	WP	0	0	0	0	0	0	0	-
91h	90h	TCS	TCS	TCS	TCS	DS	DS	RS	RS	-

Figure 8. Register Address

5.5.1、Seconds Register (Read the address: 81h, write the address: 80h)

Bit7, the highest bit of the second register, is the clock stop flag bit. If this bit is “1”, the clock crystal stops, and AiP1302 enters the low-power standby mode, with the current less than 100nA. If this bit is “0”, the crystal starts to oscillate. Bit 6~Bit 0 is 0~59 seconds.

5.5.2、Minute Register (Read the address: 83h, write the address: 82h)

The default value of Bit 7 in the register is 0, and Bit 6~Bit 0 is 0~59 minutes.

5.5.3、Hour Register (Read the address: 85h, write the address: 84h)

Hour register Bit 7 is AM/PM (12/24) mode selection bit. When “1” is set, it is 12-hour clock. When “0” is set, it is a 24-hour clock. Under the 12-hour system, Bit 5 is AM/PM flag, Bit 4~Bit 0 are 1 hour~12 hours. Under the 24-hour system, Bit 5~Bit 0 are 0 hour~23 hours.

5.5.4、Day Register (Read the address: 87h, write the address: 86h)

The default values of Bit 7 and Bit 6 of the day register are "0", and Bit 5~Bit 0 are 1 day~31 days.

5.5.5、Month Register (Read the address: 89h, write the address: 88h)

The default values of Bit 7~Bit 5 of the month register are "0". Bit 4~Bit 0 are January~December.

5.5.6、Week Register (Read the address: 8Bh, write the address: 8Ah)

The default values of Bit 7~Bit 3 of the month register are "0". Bit 2~Bit 0 are Monday~Sunday.

5.5.7、Year Register (Read the address: 8Dh, write the address: 8Ch)

In the year register, Bit 7~Bit 0 are 0 year~99 years.

5.5.8、Writing Protection Bit (Read the address: 8Fh, write the address: 8Eh)

Bit 7 is the writing protection bit，the default value of Bit6~Bit0 are "0". When Bit 7 is set to "1", it cannot be written; when it is set to "0", the writing operation can be performed.

5.5.9、Trickle Charge Register (Read the address: 91h, write the address: 90h)

Bit 7~Bit 4 of trickle charge register are trickle charge switches, which enable trickle charge only when it is set to "1010" and prohibit trickle charge for others. Bit 3 and Bit 2 are the diodes to be charged. "01" selects one diode and "10" selects two diodes. 1. Bit 1 and Bit 0 select the charge resistor, "01" is 2KΩ, "10" is 4KΩ, "11" is 8KΩ, "00" is default. The details are as follows:

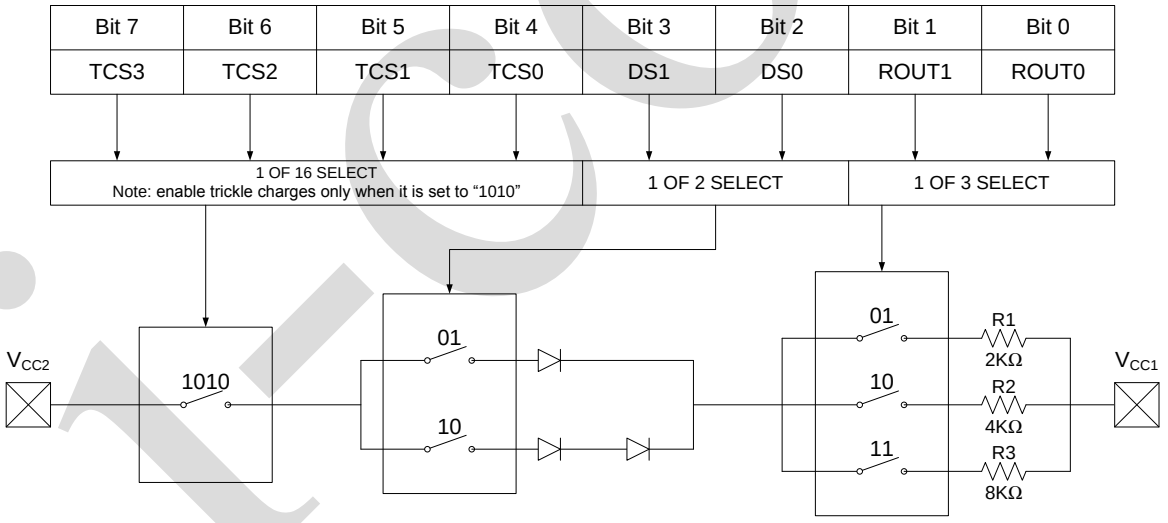


Figure 9. Current-Sharing Charging Mode

5.6、SRAM

SRAM has 31 built-in byte.

Read address	Write address	Range
C1h	C0h	00~FFh
C3h	C2h	00~FFh
…	…	…
FDh	FCh	00~FFh

5.7、Power Supply Control

V_{CC2} is the primary power supply while V_{CC1} is used as backup power supply. Even when the primary power supply is turned off, the clock can be kept running continuously. The AiP1302 is supplied by the larger one of V_{CC1} and V_{CC2}. When $V_{CC2}>V_{CC1}+0.2V$, V_{CC2} supplies power to AiP1302, and when $V_{CC2}<V_{CC1}$, AiP1302 is supplied by V_{CC1}.

6、Typical Application Circuit And Application Note

6.1、Application Circuit

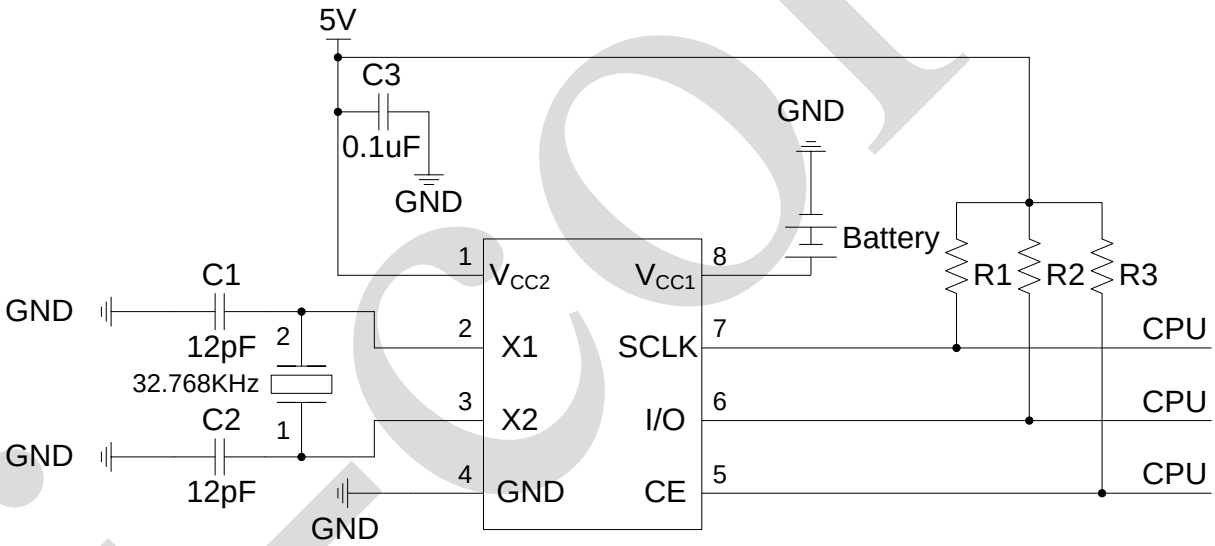


Figure 10. Typical Application Diagram

Application description:

The crystal oscillator is 32.768KHz, and the recommended starting capacitance C1 and C2 is 12pF. When the timing is inaccurate, the capacitance of C1 and C2 can be appropriately adjusted. The larger the capacitance value, the slower the timing; and the smaller the capacitance, the faster the timing.

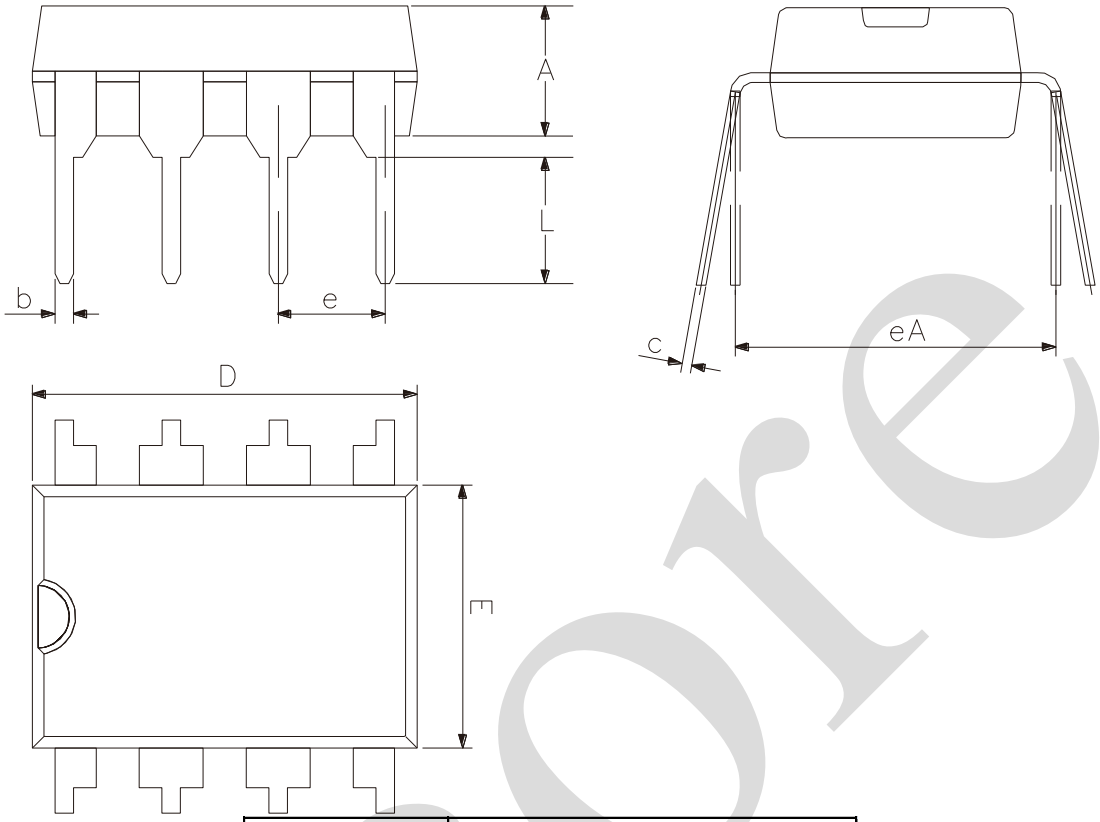
The communication port can be externally connected with a pull-up resistor to improve the communication anti-interference ability, with a resistance of 1kΩ ~ 10kΩ.

The backup power supply can be 3V button cell or large electrolytic capacitor (with small leakage), and 100uF can guarantee the normal timing of 1 hour.

AiP1302 must be initialized after being powered on for the first time, and the time can be adjusted normally after initialization.

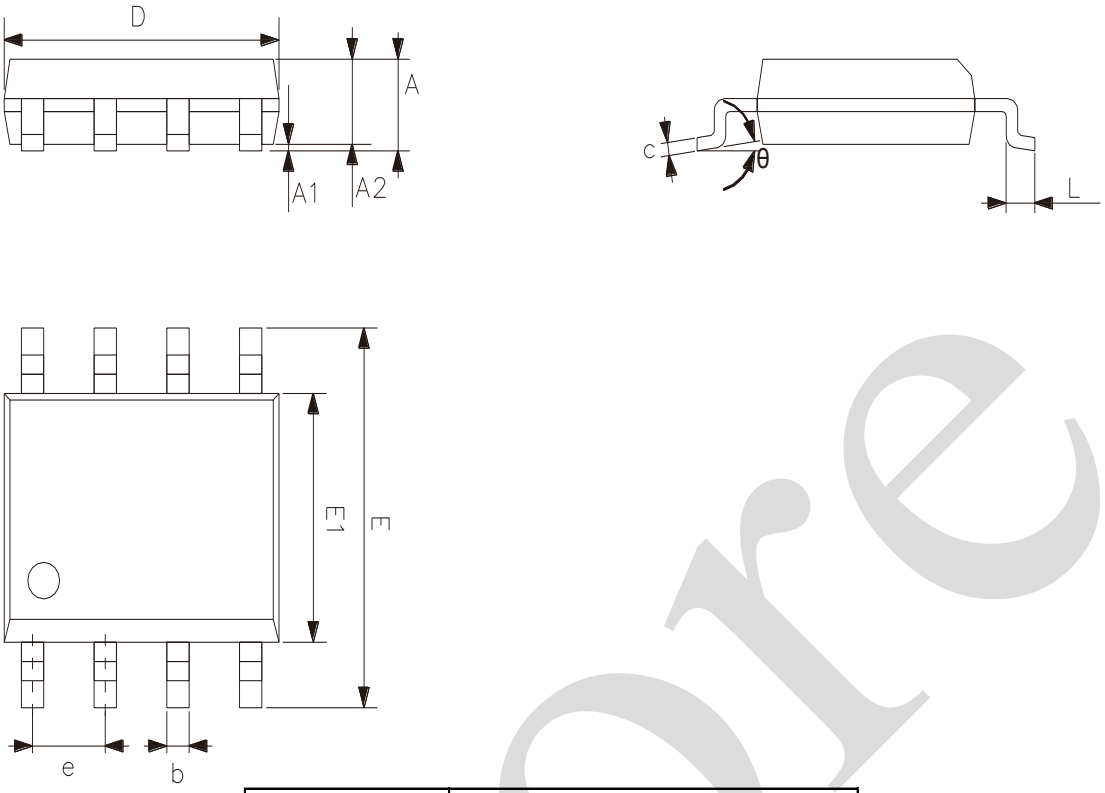
7、Package Information

7.1、DIP8



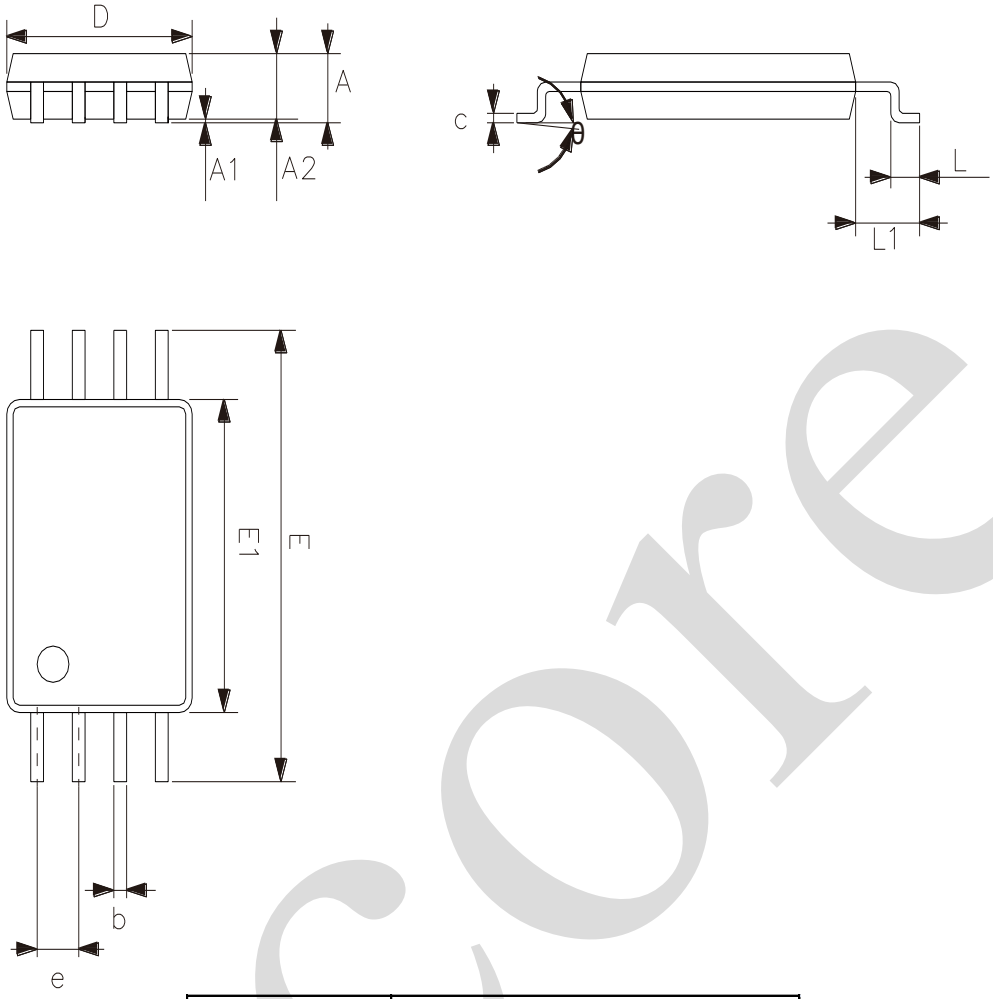
2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	3.00	3.60
b	0.36	0.56
c	0.20	0.36
D	9.00	9.45
E	6.15	6.60
e	2.54	
eA	7.62	9.30
L	3.00	—

7.2、SOP8



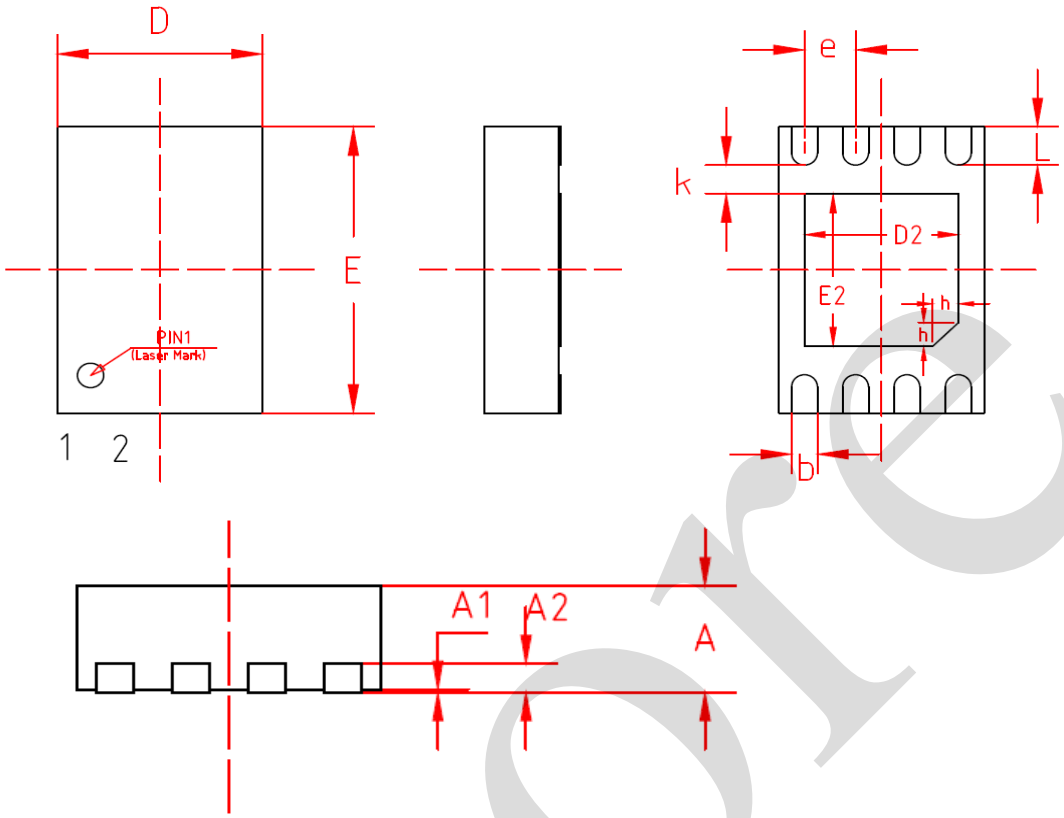
2023/12/A	Dimensions In Millimeters	
Symbol	**Min.**	**Max.**
A	1.35	1.80
A1	0.05	0.25
A2	1.25	1.55
D	4.70	5.10
E	5.80	6.30
E1	3.70	4.10
b	0.306	0.51
c	0.19	0.25
e	1.27	
L	0.40	0.89
θ	0°	8°

7.3、TSSOP8



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

7.4、DFN8



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	0.70	0.80
A1	—	0.05
A2	0.203 REF	
b	0.20	0.30
D	1.90	2.10
D2	1.40	1.60
E	2.90	3.10
E2	1.50	1.70
e	0.50	
L	0.35	0.45
h	0.20	0.30
k	0.25	0.35

8、Statements And Notes

8.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
Explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

8.2、Notes

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