AiP74LVC2G74
Single D-type flip-flop with set and reset; positive edge trigger

Product Specification

Specification Revision History:

Version	Date	Description
2017-05-A1	2017-05	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The AiP74LVC2G74 is a single positive-edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{SD}$) and reset ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable, one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Features:

- Wide supply voltage range from 1.65V to 5.5V
- 5 V tolerant outputs for interfacing with 5 V logic
- ±24mA output drive (V_{CC}=3.0V)
- CMOS low power consumption
- Latch-up performance exceeds 250mA
- Specified from -40℃ to +125℃
- Packaging information: TSSOP8/VSSOP8

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVC2G74TA8.TB	TSSOP8	ARXX	100 PCS/tube	200 tube/box	20000 PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVC2G74TA8.TR	TSSOP8	ARXX	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm
AiP74LVC2G74YA8.TR	VSSOP8	ARXX	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 2.0mm×2.3mm Pin spacing:0.50mm

Note 1: "XX" refers to variable content, meaning year and package batch serial number.

Note 2: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

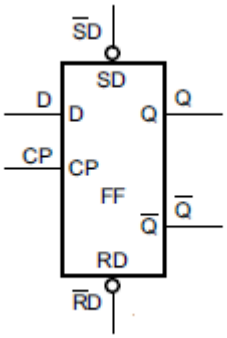


Figure 1. Logic symbol

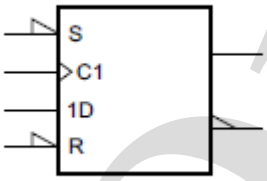


Figure 2. IEC logic symbol

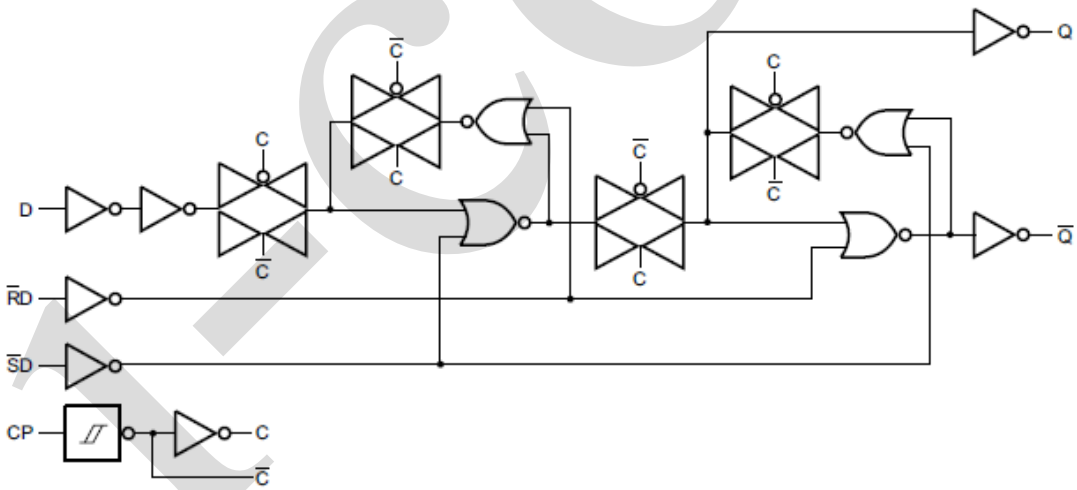
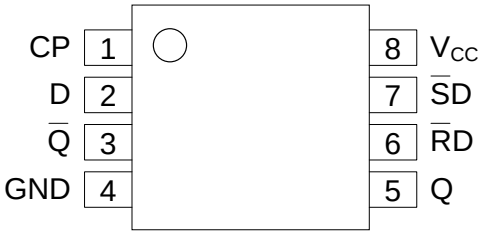


Figure 3. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	D	data input
3	$\overline{Q}$	complement output
4	GND	ground (0V)
5	Q	true output
6	$\overline{RD}$	asynchronous reset-direct input (active LOW)
7	$\overline{SD}$	asynchronous set-direct input (active LOW)
8	V_{CC}	supply voltage

2.4、Function Table

Function table for asynchronous operation

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Note: H=HIGH voltage level; L=LOW voltage level; X=don’t care.

Function table for synchronous operation

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

Note: H=HIGH voltage level; L=LOW voltage level; ↑=LOW-to-HIGH CP transition;
Q_{n+1}=state after the next LOW-to-HIGH CP transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+6.5	V
input clamping current	I_{IK}	$V_I < 0V$	-50	-	mA
input voltage	V_I	-	-0.5	+6.5	V
output clamping current	I_{OK}	$V_O > V_{CC}$ or $V_O < 0V$	-	±50	mA
output voltage	V_O	Active mode	-0.5	V_{CC}+0.5	V
		Power-down mode; V_{CC}=0V	-0.5	+6.5	V
output current	I_O	V_O=0V to V_{CC}	-	±50	mA
supply current	I_{CC}	-	-	100	mA
ground current	I_{GND}	-	-100	-	mA
total power dissipation	P_{tot}	-	-	300	mW
storage temperature	T_{stg}	-	-65	+150	℃
Soldering temperature	T_L	10s	260		℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	1.65	-	5.5	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC}=0V	0	-	5.5	V
ambient temperature	T_{amb}	-	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.65V to 1.95V		0.65× V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7× V_{CC}	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.65V to 1.95V		-	-	0.35× V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3× V_{CC}	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	V_{CC}-0.1	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.2	1.54	-	V
			I_O=-8mA; V_{CC}=2.3V	1.9	2.15	-	V
			I_O=-12mA; V_{CC}=2.7V	2.2	2.50	-	V
			I_O=-24mA; V_{CC}=3.0V	2.3	2.62	-	V
			I_O=-32mA; V_{CC}=4.5V	3.8	4.11	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 5.5V	-	-	0.10	V
			I_O=4mA; V_{CC}=1.65V	-	0.07	0.45	V
			I_O=8mA; V_{CC}=2.3V	-	0.12	0.30	V
			I_O=12mA; V_{CC}=2.7V	-	0.17	0.40	V
			I_O=24mA; V_{CC}=3.0V	-	0.33	0.55	V
			I_O=32mA; V_{CC}=4.5V	-	0.39	0.55	V
input leakage current	I_I	V_I=5.5V or GND; V_{CC}=0V to 5.5V		-	-	±1	uA
power-off leakage current	I_{OFF}	V_I or V_O=5.5V; V_{CC}=0V		-	-	±2	uA
supply current	I_{CC}	V_I=5.5V or GND; I_O=0A; V_{CC}=1.65V to 5.5V		-	-	4	uA
additional supply current	ΔI_{CC}	per pin; V_I=V_{CC}-0.6V; I_O=0A; V_{CC}=2.3V to 5.5V		-	-	500	uA
input capacitance	C_I	-		-	4.0	-	pF

Note: All typical values are measured at T_{amb}=25℃.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.65V to 1.95V		0.65× V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7× V_{CC}	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.65V to 1.95V		-	-	0.35× V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3× V_{CC}	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	V_{CC}-0.1	-	-	V
			I_O=-4mA; V_{CC}=1.65V	0.95	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.7	-	-	V
			I_O=-12mA; V_{CC}=2.7V	1.9	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.0	-	-	V
			I_O=-32mA; V_{CC}=4.5V	3.4	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 5.5V	-	-	0.10	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.70	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.45	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.60	V
			I_O=24mA; V_{CC}=3.0V	-	-	0.80	V
			I_O=32mA; V_{CC}=4.5V	-	-	0.80	V
input leakage current	I_I	V_I=5.5V or GND; V_{CC}=0V to 5.5V		-	-	±1	uA
power-off leakage current	I_{OFF}	V_I or V_O=5.5V; V_{CC}=0V		-	-	±2	uA
supply current	I_{CC}	V_I=5.5V or GND; I_O=0A; V_{CC}=1.65V to 5.5V		-	-	4	uA
additional supply current	ΔI_{CC}	per pin; V_I=V_{CC}-0.6V; I_O=0A; V_{CC}=2.3V to 5.5V		-	-	500	uA

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
propagation delay	t_{PHL}	CP to Q, $\overline{Q}$; see Figure 5	V_{CC}=1.65V to 1.95V	-	12.5	18.8	ns
			V_{CC}=2.3V to 2.7V	-	10.5	15.8	ns
			V_{CC}=2.7V	-	10	15	ns
			V_{CC}=3.0V to 3.6V	-	9.5	14.3	ns
			V_{CC}=4.5V to 5.5V	-	9	13.5	ns
		$\overline{SD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	-	12.5	18.8	ns
			V_{CC}=2.3V to 2.7V	-	10.5	15.8	ns
			V_{CC}=2.7V	-	10	15	ns
			V_{CC}=3.0V to 3.6V	-	9.5	14.3	ns
			V_{CC}=4.5V to 5.5V	-	9	13.5	ns
		$\overline{RD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	-	12.5	18.8	ns
			V_{CC}=2.3V to 2.7V	-	10.5	15.8	ns
			V_{CC}=2.7V	-	10	15	ns
			V_{CC}=3.0V to 3.6V	-	9.5	14.3	ns
			V_{CC}=4.5V to 5.5V	-	9	13.5	ns
propagation delay	t_{PLH}	CP to Q, $\overline{Q}$; see Figure 5	V_{CC}=1.65V to 1.95V	-	14	21	ns
			V_{CC}=2.3V to 2.7V	-	10	15	ns
			V_{CC}=2.7V	-	9.5	14.3	ns
			V_{CC}=3.0V to 3.6V	-	8.5	12.8	ns
			V_{CC}=4.5V to 5.5V	-	7.5	11.3	ns
		$\overline{SD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	-	14	21	ns
			V_{CC}=2.3V to 2.7V	-	10	15	ns
			V_{CC}=2.7V	-	9.5	14.3	ns
			V_{CC}=3.0V to 3.6V	-	8.5	12.8	ns
			V_{CC}=4.5V to 5.5V	-	7.5	11.3	ns
		$\overline{RD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	-	14	21	ns
			V_{CC}=2.3V to 2.7V	-	10	15	ns
			V_{CC}=2.7V	-	9.5	14.3	ns
			V_{CC}=3.0V to 3.6V	-	8.5	12.8	ns
			V_{CC}=4.5V to 5.5V	-	7.5	11.3	ns
pulse width	t_W	CP HIGH or LOW; see Figure 5	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	1.3	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
		$\overline{SD}$ and $\overline{RD}$ LOW; see Figure 6	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	1.6	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
recovery time	t_{rec}	$\overline{SD}$ or $\overline{RD}$; see Figure 6	V_{CC}=1.65V to 1.95V	1.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.4	-	-	ns

			V_{CC}=2.7V	1.3	-	-	ns
			V_{CC}=3.0V to 3.6V	+1.2	-3.0	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
set-up time	t_{su}	D to CP; see Figure 5	V_{CC}=1.65V to 1.95V	2.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.7	-	-	ns
			V_{CC}=2.7V	1.7	-	-	ns
			V_{CC}=3.0V to 3.6V	1.3	0.5	-	ns
			V_{CC}=4.5V to 5.5V	1.1	-	-	ns
hold time	t_h	D to CP; see Figure 5	V_{CC}=1.65V to 1.95V	1.5	-	-	ns
			V_{CC}=2.3V to 2.7V	1.0	-	-	ns
			V_{CC}=2.7V	1.0	-	-	ns
			V_{CC}=3.0V to 3.6V	1.0	0.6	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 5	V_{CC}=1.65V to 1.95V	80	-	-	MHz
			V_{CC}=2.3V to 2.7V	175	-	-	MHz
			V_{CC}=2.7V	175	-	-	MHz
			V_{CC}=3.0V to 3.6V	175	280	-	MHz
			V_{CC}=4.5V to 5.5V	200	-	-	MHz
Power dissipation capacitance	C_{PD}	V_{CC}=3.3V; V_I=GND to V_{CC}		-	15	-	pF

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.8V, 2.5V, 2.7V, 3.3V and 5.0V respectively.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{PHL}	CP to Q, $\overline{Q}$; see Figure 5	V_{CC}=1.65V to 1.95V	-	-	20.8	ns
			V_{CC}=2.3V to 2.7V	-	-	17.8	ns
			V_{CC}=2.7V	-	-	17	ns
			V_{CC}=3.0V to 3.6V	-	-	16.3	ns
			V_{CC}=4.5V to 5.5V	-	-	15.5	ns
		$\overline{SD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	-	-	20.8	ns
			V_{CC}=2.3V to 2.7V	-	-	17.8	ns
			V_{CC}=2.7V	-	-	17	ns
			V_{CC}=3.0V to 3.6V	-	-	16.3	ns
			V_{CC}=4.5V to 5.5V	-	-	15.5	ns
		$\overline{RD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	-	-	20.8	ns
			V_{CC}=2.3V to 2.7V	-	-	17.8	ns
			V_{CC}=2.7V	-	-	17	ns
			V_{CC}=3.0V to 3.6V	-	-	16.3	ns
			V_{CC}=4.5V to 5.5V	-	-	15.5	ns
propagation delay	t_{PLH}	CP to Q, $\overline{Q}$; see Figure 5	V_{CC}=1.65V to 1.95V	-	-	23	ns
			V_{CC}=2.3V to 2.7V	-	-	17	ns
			V_{CC}=2.7V	-	-	16.3	ns

			V_{CC}=3.0V to 3.6V	-	-	14.8	ns
			V_{CC}=4.5V to 5.5V	-	-	13.3	ns
		$\overline{SD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	-	-	23	ns
			V_{CC}=2.3V to 2.7V	-	-	17	ns
			V_{CC}=2.7V	-	-	16.3	ns
			V_{CC}=3.0V to 3.6V	-	-	14.8	ns
			V_{CC}=4.5V to 5.5V	-	-	13.3	ns
		$\overline{RD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	-	-	23	ns
			V_{CC}=2.3V to 2.7V	-	-	17	ns
			V_{CC}=2.7V	-	-	16.3	ns
			V_{CC}=3.0V to 3.6V	-	-	14.8	ns
			V_{CC}=4.5V to 5.5V	-	-	13.3	ns
pulse width	t_W	CP HIGH or LOW; see Figure 5	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	-	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
		$\overline{SD}$ and $\overline{RD}$ LOW; see Figure 6	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	-	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
recovery time	t_{rec}	$\overline{SD}$ or $\overline{RD}$; see Figure 6	V_{CC}=1.65V to 1.95V	1.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.4	-	-	ns
			V_{CC}=2.7V	1.3	-	-	ns
			V_{CC}=3.0V to 3.6V	+1.2	-	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
set-up time	t_{su}	D to CP; see Figure 5	V_{CC}=1.65V to 1.95V	2.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.7	-	-	ns
			V_{CC}=2.7V	1.7	-	-	ns
			V_{CC}=3.0V to 3.6V	1.3	-	-	ns
			V_{CC}=4.5V to 5.5V	1.1	-	-	ns
hold time	t_h	D to CP; see Figure 5	V_{CC}=1.65V to 1.95V	1.5	-	-	ns
			V_{CC}=2.3V to 2.7V	1.0	-	-	ns
			V_{CC}=2.7V	1.0	-	-	ns
			V_{CC}=3.0V to 3.6V	1.0	-	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 5	V_{CC}=1.65V to 1.95V	80	-	-	MHz
			V_{CC}=2.3V to 2.7V	175	-	-	MHz
			V_{CC}=2.7V	175	-	-	MHz
			V_{CC}=3.0V to 3.6V	175	-	-	MHz
			V_{CC}=4.5V to 5.5V	200	-	-	MHz

4、Testing Circuit

4.1、AC Testing Circuit

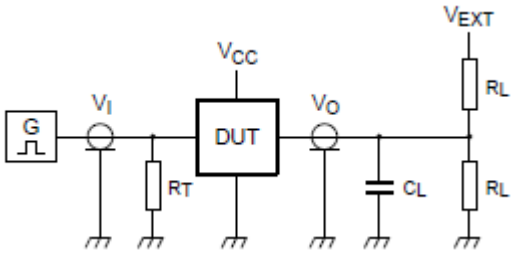


Figure 4. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance; should be equal to the output impedance Z_o of the pulse generator.

V_{EXT}=External voltage for measuring switching times.

4.2、AC Testing Waveforms

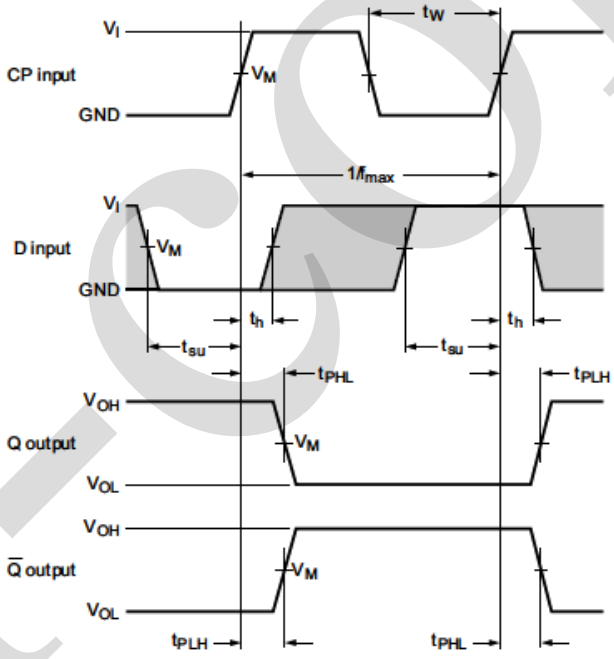


Figure 5. The clock input (CP) to output (Q, $\overline{Q}$) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times and the maximum frequency

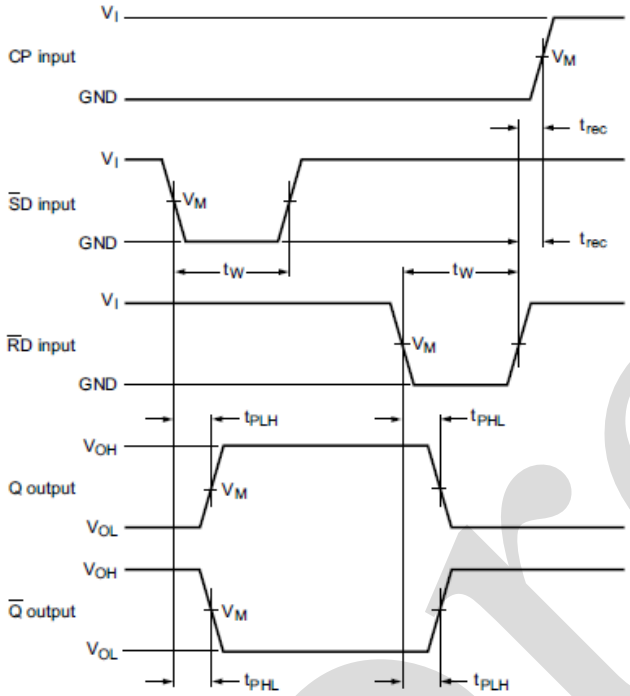


Figure 6. The set ($\overline{SD}$) and reset ($\overline{RD}$) input to output (Q, $\overline{Q}$) propagation delays, the set and reset pulse widths and the $\overline{RD}$ to CP recovery time

4.3、Measurement Points

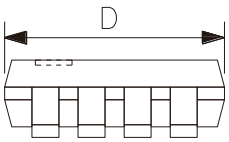
Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65V to 1.95V	$0.5\times V_{CC}$	$0.5\times V_{CC}$
2.3V to 2.7V	$0.5\times V_{CC}$	$0.5\times V_{CC}$
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	$0.5\times V_{CC}$	$0.5\times V_{CC}$

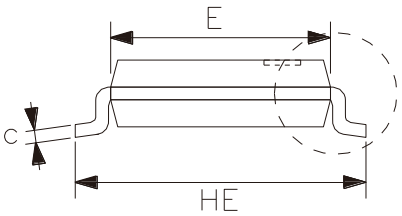
4.4、Test Data

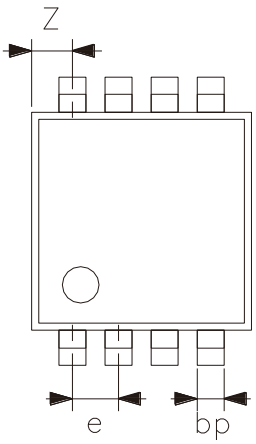
Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65V to 1.95V	V_{CC}	≤ 3ns	30pF	1kΩ	open	GND	$2\times V_{CC}$
2.3V to 2.7V	V_{CC}	≤ 3ns	30pF	500Ω	open	GND	$2\times V_{CC}$
2.7V	2.7V	≤ 3ns	50pF	500Ω	open	GND	6V
3.0V to 3.6V	2.7V	≤ 3ns	50pF	500Ω	open	GND	6V
4.5V to 5.5V	V_{CC}	≤ 3ns	50pF	500Ω	open	GND	$2\times V_{CC}$

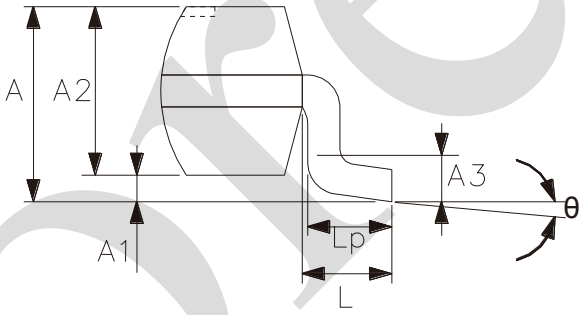
5、Package Information

5.1、TSSOP8



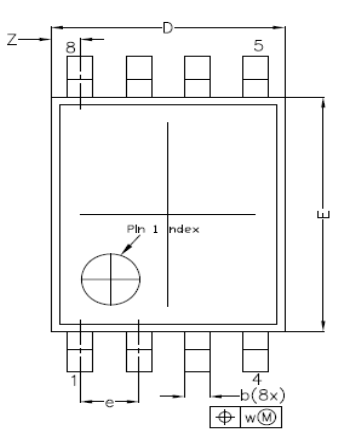




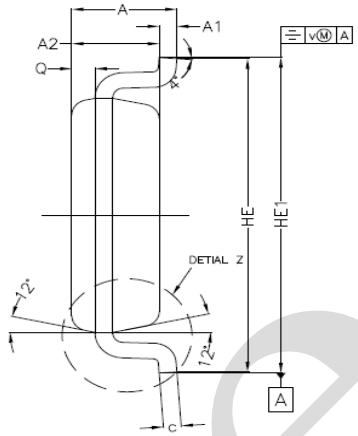


Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.10
A1	0	0.15
A2	0.75	0.95
A3	0.25	
bp	0.22	0.38
c	0.08	0.18
D	2.90	3.10
E	2.90	3.10
HE	3.90	4.10
L	0.50	
Lp	0.33	0.47
e	0.65	
Z	0.35	0.70
θ	0°	8°

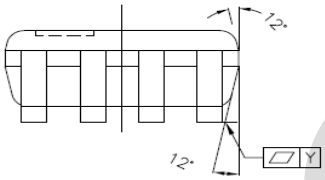
5.2、VSSOP8



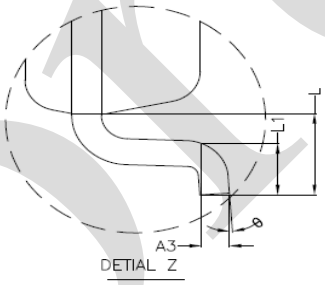
TOP VIEW



SIDE VIEW



SIDE VIEW



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.00
A1	0.00	0.15
A2	0.60	0.85
A3	0.12	
Q	0.19	0.21
b	0.17	0.27
c	0.08	0.23
D	1.90	2.10
E	2.20	2.40
HE	3.00	3.20
HE1	3.00	3.40
e	0.50	
L	0.40	
L1	0.15	0.40
Y	0.10	
Z	0.10	0.40
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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