AiP74LVC32
Quad 2-input Or Gate

Product Specification

Specification Revision History：

Version	Date	Description
2017-05-A1	2017-05	New
2023-04-B1	2023-04	Update the template
2025-05-B2	2025-05	Add VQFN14 package form
2025-12-B3	2025-12	Modify the supply voltage range; add the parameters at the condition of V_{CC}=4.5V to 5.5V; add ESD

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1、General Description

The AiP74LVC32 provides four 2-input OR gates.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V applications.

Features:

- 5V tolerant inputs for interfacing with 5V logic
- Wide supply voltage range from 1.2V to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Specified from -40℃ to +125℃
- Packaging information: DIP14/SOP14/TSSOP14/VQFN14

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Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVC32DA14.TB	DIP14	74LVC32	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74LVC32SA14.TB	SOP14	74LVC32	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74LVC32TA14.TB	TSSOP14	74LVC32	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVC32SA14.TR	SOP14	74LVC32	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74LVC32TA14.TR	TSSOP14	74LVC32	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74LVC32QK14.TR	VQFN14	74LVC32	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 3.5mm×3.5mm 3in spacing: 0.50mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

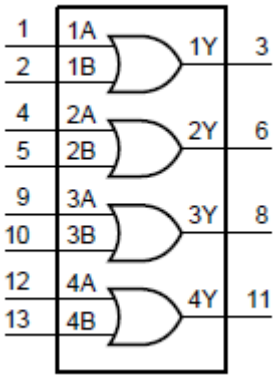


Figure 1. Logic symbol

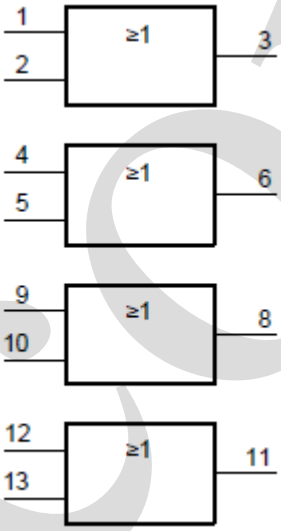


Figure 2. IEC logic symbol

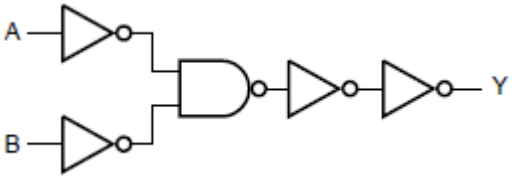
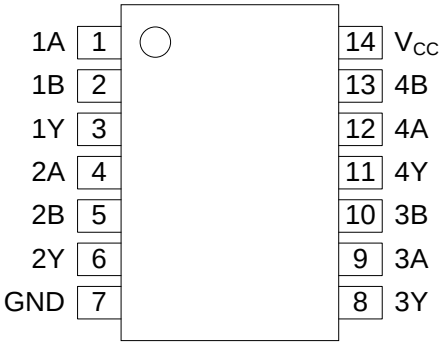
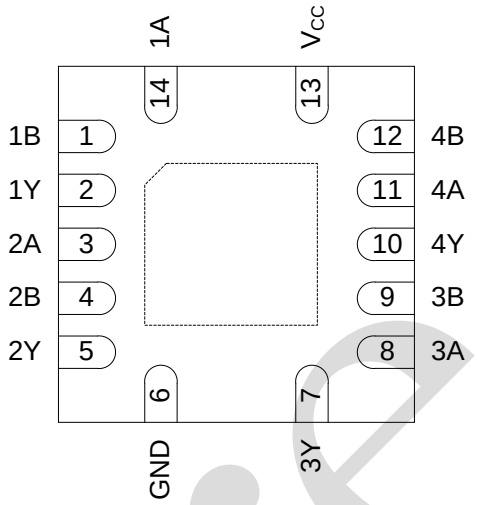


Figure 3. Logic diagram for one gate

2.2、Pin Configurations



DIP14/SOP14/TSSOP14



VQFN14

2.3、Pin Description

Pin No.		Pin Name	Description
DIP14/SOP14/TSSOP14	VQFN14		
1	14	1A	data input
2	1	1B	data input
3	2	1Y	data output
4	3	2A	data input
5	4	2B	data input
6	5	2Y	data output
7	6	GND	ground (0V)
8	7	3Y	data output
9	8	3A	data input
10	9	3B	data input
11	10	4Y	data output
12	11	4A	data input
13	12	4B	data input
14	13	V_{CC}	supply voltage

2.4、Function Table

Input		Output
nA	nB	nY
L	L	L
X	H	H
H	X	H

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+6.5	V
input clamping current	I_{IK}	$V_I < 0V$		-50	-	mA
input voltage	V_I	-		-0.5	+6.5	V
output clamping current	I_{OK}	$V_O > V_{CC}$ or $V_O < 0V$		-	±50	mA
output voltage	V_O	-		-0.5	V_{CC}+0.5	V
output current	I_O	V_O=0V to V_{CC}		-	±50	mA
supply current	I_{CC}	-		-	100	mA
ground current	I_{GND}	-		-100	-	mA
total power dissipation	P_{tot}	-		-	500	mW
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP/VQFN	260		
electrostatic discharge	ESD	HBM		2000		V

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	1.65	-	5.5	V
		functional	1.2	-	-	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃
input transition rise and fall rate	$\Delta t/\Delta V$	V_{CC}=1.65V to 2.7V	0	-	20	ns/V
		V_{CC}=2.7V to 3.6V	0	-	10	ns/V

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3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65× V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7× V_{CC}	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35× V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3× V_{CC}	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	V_{CC} - 0.2	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.2	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.8	-	-	V
			I_O=-12mA; V_{CC}=2.7V	2.2	-	-	V
			I_O=-18mA; V_{CC}=3.0V	2.4	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.2	-	-	V
			I_O=-32mA; V_{CC}=4.5V	3.8	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 5.5V	-	-	0.2	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.45	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.6	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.4	V
			I_O=24mA; V_{CC}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CC}=4.5V	-	-	0.55	V
input leakage current	I_I	V_I=5.5V or GND; V_{CC}=3.6V		-	-	±5	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=3.6V		-	-	15	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-0.6V; I_O=0A; V_{CC}=2.7V to 3.6V		-	-	500	uA
input capacitance	C_I	V_{CC}=0V to 3.6V; V_I= GND to V_{CC}		-	4.0	-	pF

Note: All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65× V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7× V_{CC}	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35× V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3× V_{CC}	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	V_{CC} - 0.3	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.05	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.65	-	-	V
			I_O=-12mA; V_{CC}=2.7V	2.05	-	-	V
			I_O=-18mA; V_{CC}=3.0V	2.25	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.0	-	-	V
			I_O=-32mA; V_{CC}=4.5V	3.4	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 5.5V	-	-	0.3	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.65	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.8	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.6	V
			I_O=24mA; V_{CC}=3.0V	-	-	0.8	V
			I_O=32mA; V_{CC}=4.5V	-	-	0.8	V
input leakage current	I_I	V_I=5.5V or GND; V_{CC}=3.6V		-	-	±20	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=3.6V		-	-	200	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-0.6V; I_O=0A; V_{CC}=2.7V to 3.6V		-	-	5000	uA

Note: All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
nA, nB to nY propagation delay	t_{pd}	see Figure 5	V_{CC}=1.2V	-	10	-	ns
			V_{CC}=1.65V to 1.95V	0.5	4.2	9.0	ns
			V_{CC}=2.3V to 2.7V	1.5	2.4	4.9	ns
			V_{CC}=2.7V	1.5	2.5	4.4	ns
			V_{CC}=3.0V to 3.6V	1.0	2.2	3.8	ns
			V_{CC}=4.5V to 5.5V	1.0	1.9	3.3	ns
output skew time	$t_{sk(o)}$	V_{CC}=3.0V to 3.6V		-	-	1.0	ns
power dissipation capacitance	C_{PD}	per gate; V_I=GND to V_{CC}	V_{CC}=1.65V to 1.95V	-	4.7	-	pF
			V_{CC}=2.3V to 2.7V	-	8.0	-	pF
			V_{CC}=3.0V to 3.6V	-	11.0	-	pF

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.2V, 1.8V, 2.5V, 2.7V and 3.3V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
nA, nB to nY propagation delay	t_{pd}	see Figure 5	V_{CC}=1.65V to 1.95V	0.5	-	10.4	ns
			V_{CC}=2.3V to 2.7V	1.5	-	5.7	ns
			V_{CC}=2.7V	1.5	-	5.5	ns
			V_{CC}=3.0V to 3.6V	1.0	-	5.0	ns
			V_{CC}=4.5V to 5.5V	1.0	-	4.3	ns
output skew time	$t_{sk(o)}$	V_{CC}=3.0V to 3.6V		-	-	1.5	ns

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.2V, 1.8V, 2.5V, 2.7V and 3.3V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

4、Testing Circuit

4.1、AC Testing Circuit

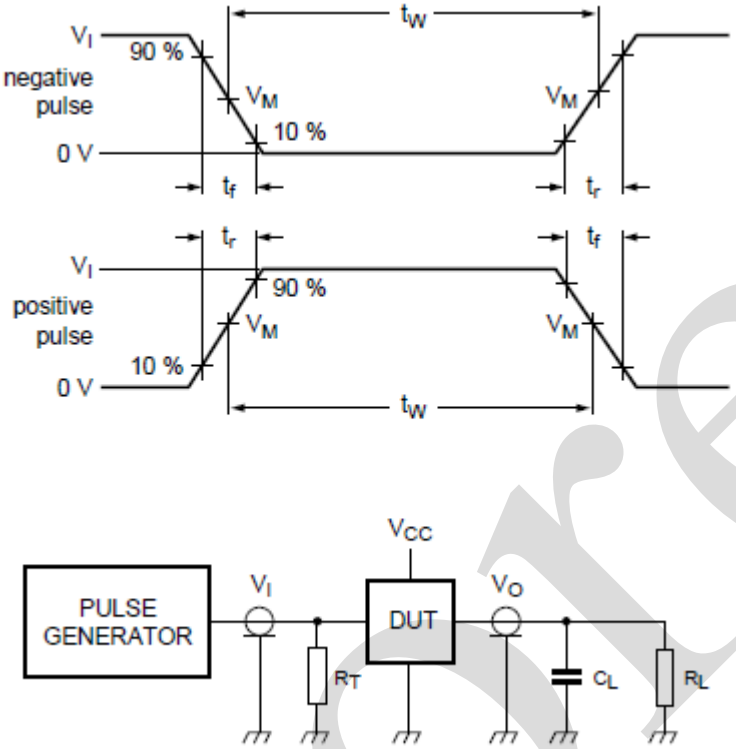

Figure 4. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

4.2、AC Testing Waveforms

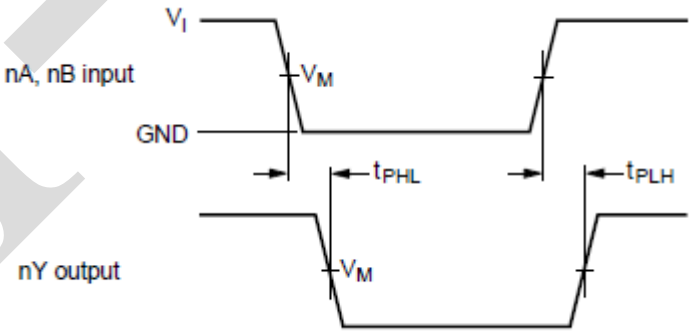

Figure 5. The input (nA, nB) to output (nY) propagation delays

4.3、Measurement Points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
≥ 2.7V	1.5V	1.5V

4.4、Test Data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r , t_f	C_L	R_L
1.2V	V_{CC}	≤ 2.0ns	30pF	1kΩ
1.65V to 1.95V	V_{CC}	≤ 2.0ns	30pF	1kΩ
2.3V to 2.7V	V_{CC}	≤ 2.0ns	30pF	500Ω
2.7V	2.7V	≤ 2.5ns	50pF	500Ω
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω

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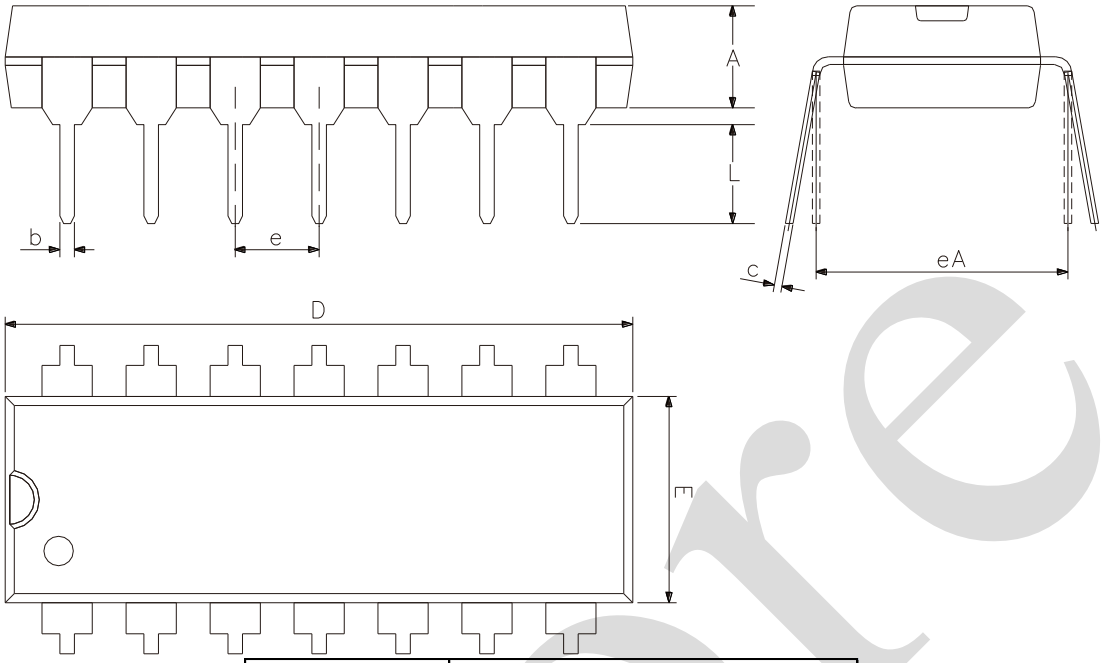
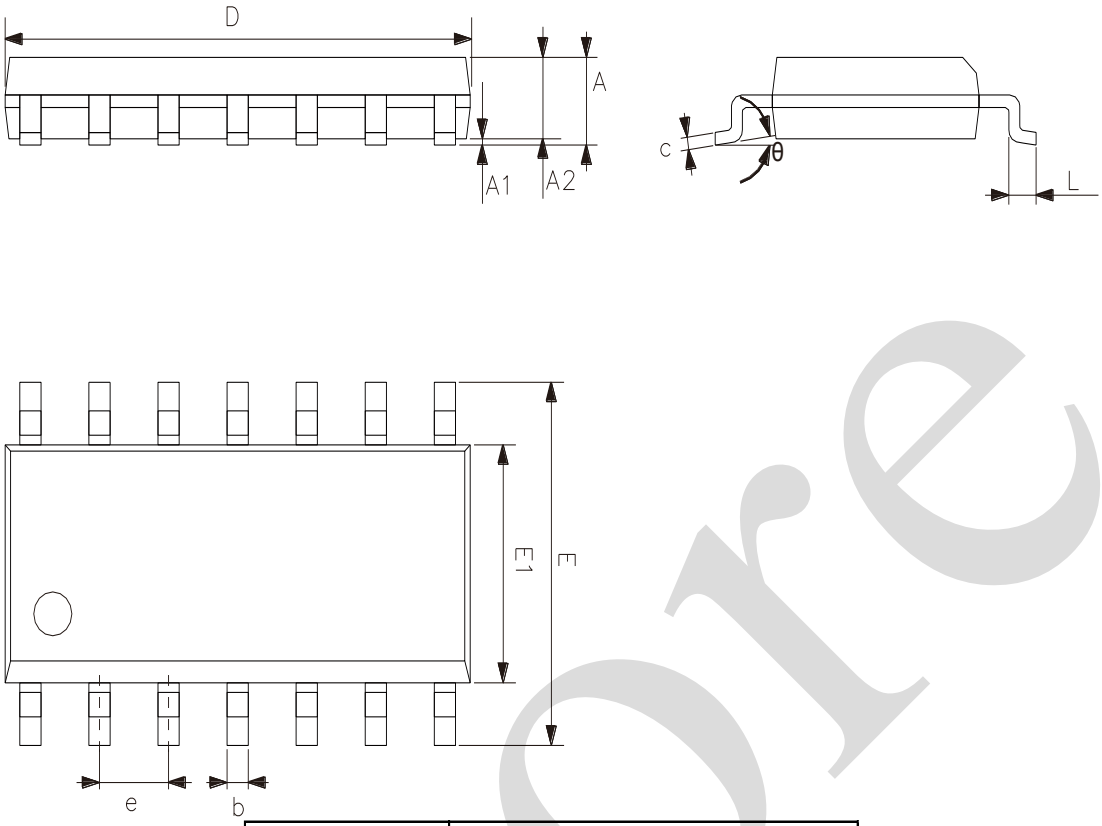
5、Package Information

5.1、DIP14



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	3.05	3.60
b	0.33	0.56
c	0.20	0.36
D	18.80	19.40
E	6.20	6.60
e	2.54	
eA	7.62	10.90
L	2.92	—

5.2、SOP14



2023/12/A	Dimensions In Millimeters	
Symbol	**Min.**	**Max.**
A	1.50	1.75
A1	0.05	0.25
A2	1.30	—
b	0.33	0.50
c	0.19	0.25
D	8.43	8.76
E	5.80	6.25
E1	3.75	4.00
e	1.27	
L	0.40	0.89
θ	0°	8°

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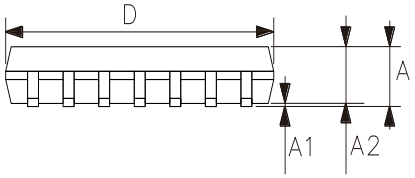
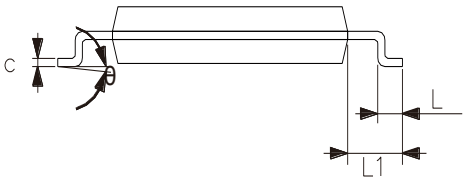
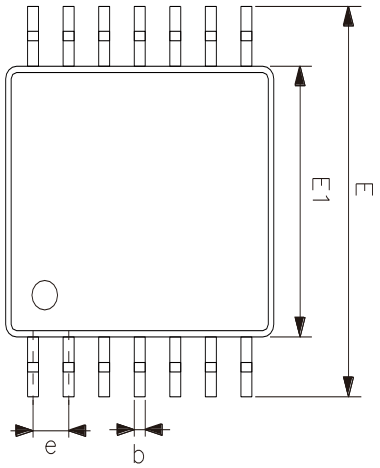
5.3、TSSOP14

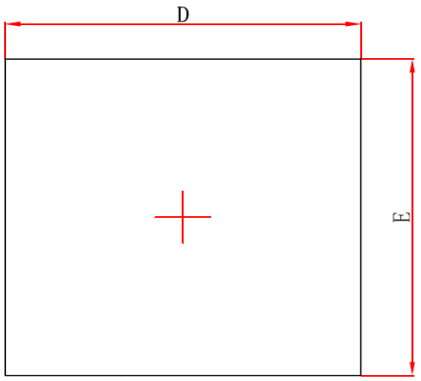




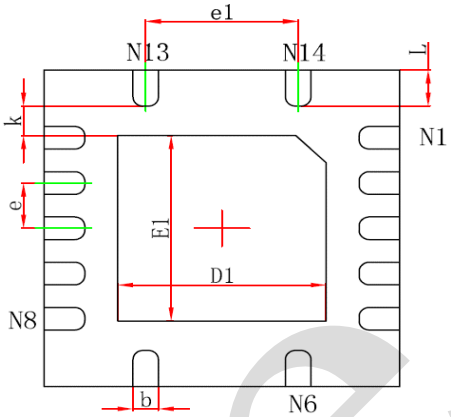


2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

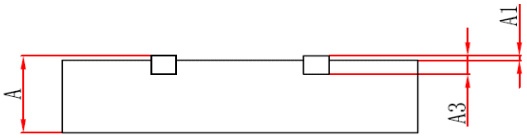
5.4、VQFN14



Top View



Bottom View



Side View

2024/08/A	Dimensions In Millimeters	
Symbol	Min	Max
A	0.70	0.90
A1	0	0.05
A3	0.203 REF	
D	3.424	3.576
E	3.424	3.576
D1	1.95	2.15
E1	1.95	2.15
k	0.20	—
b	0.20	0.30
e	0.50	
e1	1.50	
L	0.324	0.476

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We Recommend you to read this chapter carefully before using this product.

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