



AiP74AVC16T245

16-bit Dual Supply Translating Transceiver; 3-state

Product Specification

Specification Revision History:

Version	Date	Description
2019-03-A1	2019-03	New
2023-04-B1	2023-04	Update the template



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1、General Description

The AiP74AVC16T245 is a 16-bit transceiver with bidirectional level voltage translation and 3-state outputs. The device can be used as two 8-bit transceivers or as a 16-bit transceiver. It has dual supplies ($V_{CC(A)}$ and $V_{CC(B)}$) for voltage translation and four 8-bit input-output ports (nAn and nBn) each with its own output enable ($\overline{nOE}$) and send/receive (nDIR) input for direction control. $V_{CC(A)}$ and $V_{CC(B)}$ can be independently supplied at any voltage between 0.8V and 3.6V making the device suitable for low voltage translation between any of the following voltages: 0.8V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V. A HIGH on nDIR selects transmission from nAn to nBn while a LOW on nDIR selects transmission from nBn to nAn. A

HIGH on $\overline{nOE}$ causes the outputs to assume a high-impedance OFF-state

The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both nAn and nBn are in the high-impedance OFF-state.

Features:

- Wide supply voltage range:
 $V_{CC(A)}$: 0.8V to 3.6V
 $V_{CC(B)}$: 0.8V to 3.6V
- Maximum data rates:
380 Mbit/s ($\geq 1.8V$ to 3.3V translation)
200 Mbit/s ($\geq 1.1V$ to 3.3V translation)
200 Mbit/s ($\geq 1.1V$ to 2.5V translation)
200 Mbit/s ($\geq 1.1V$ to 1.8V translation)
150 Mbit/s ($\geq 1.1V$ to 1.5V translation)
100 Mbit/s ($\geq 1.1V$ to 1.2V translation)
- Suspend mode
- Inputs accept voltages up to 3.6V
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from $-40^{\circ}C$ to $+125^{\circ}C$
- Packaging information: TSSOP48

**Ordering Information:****Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74AVC16T245 TA48.TB	TSSOP48	74AVC16T245	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74AVC16T245 TA48.TR	TSSOP48	74AVC16T245	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing:0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

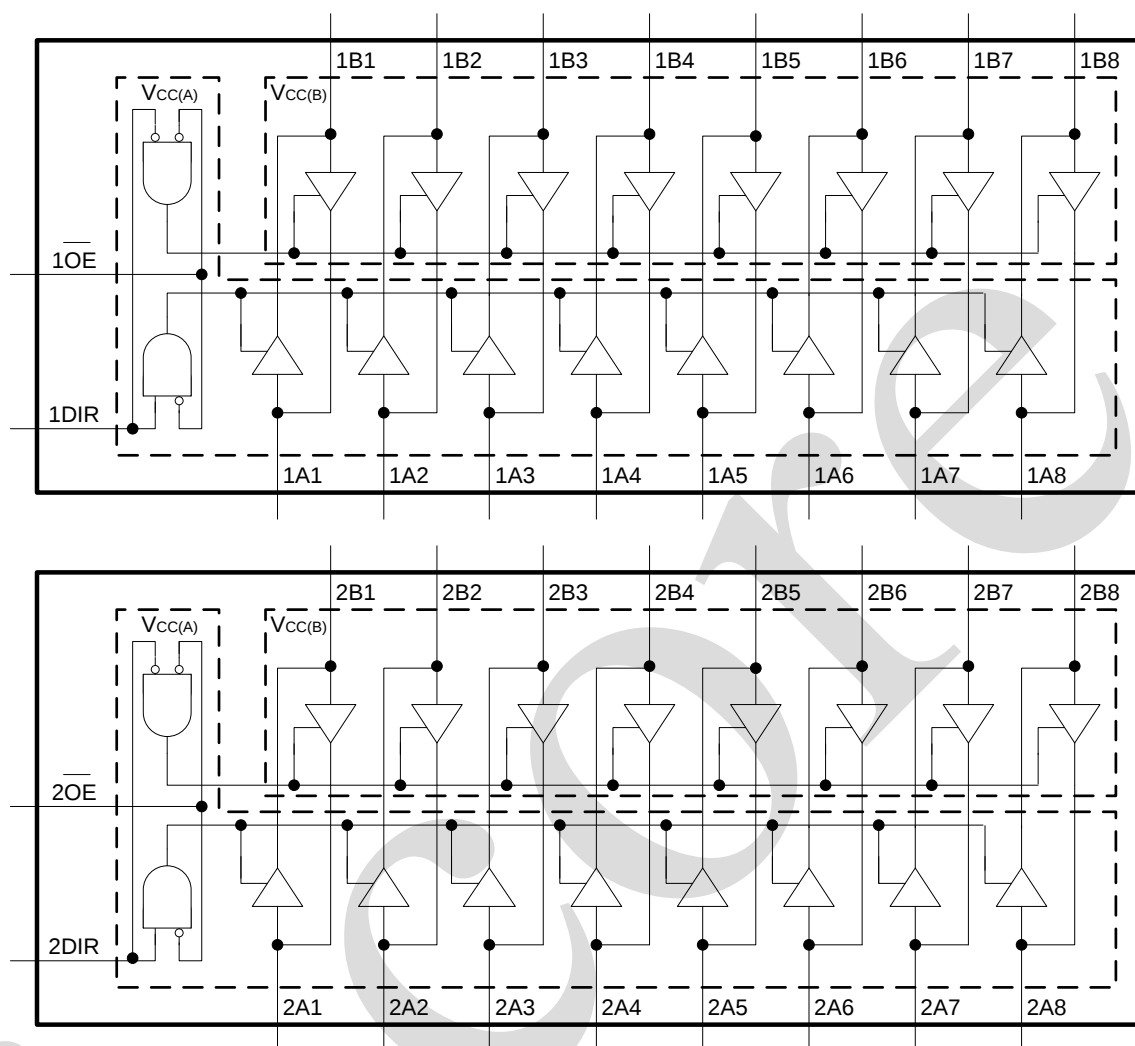


Figure 1. Logic symbol

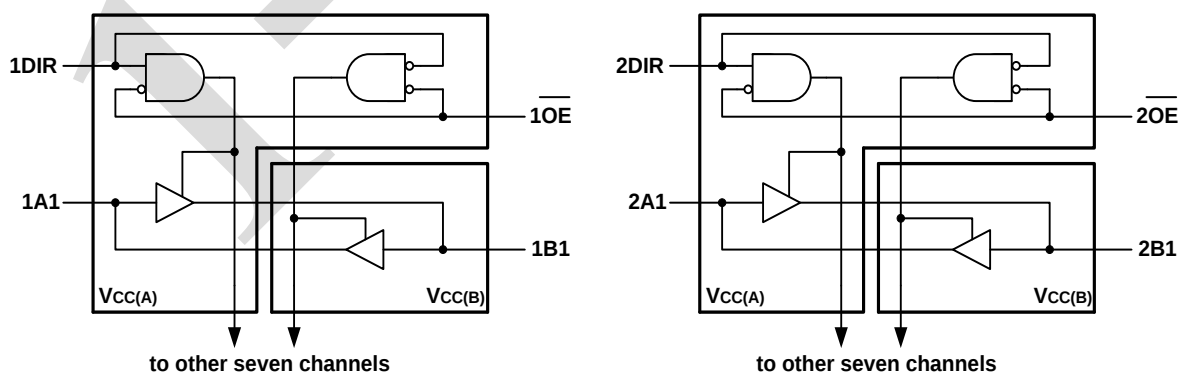


Figure 2. Logic diagram



2.2、Pin Configurations

1	1DIR	1OE	48
2	1B1	1A1	47
3	1B2	1A2	46
4	GND	GND	45
5	1B3	1A3	44
6	1B4	1A4	43
7	VCC(B)	VCC(A)	42
8	1B5	1A5	41
9	1B6	1A6	40
10	GND	GND	39
11	1B7	1A7	38
12	1B8	1A8	37
13	2B1	2A1	36
14	2B2	2A2	35
15	GND	GND	34
16	2B3	2A3	33
17	2B4	2A4	32
18	VCC(B)	VCC(A)	31
19	2B5	2A5	30
20	2B6	2A6	29
21	GND	GND	28
22	2B7	2A7	27
23	2B8	2A8	26
24	2DIR	2OE	25

2.3、Pin Description

Pin No.	Pin Name	Description
1,24	1DIR,2 DIR	direction control
2,3,5,6,8,9,11,12	1B1,1B2,1B3,1B4,1B5,1B6,1B7,1B8	data input or output
13,14,16,17,19,20,22,23	2B1,2B2,2B3,2B4,2B5,2B6,2B7,2B8	data input or output
4,10,15,21,28,34,39,45	GND ^[1]	ground (0V)
7,18	V _{CC(B)}	supply voltage B (nBn inputs/outputs are referenced to V _{CC(B)})
48,25	1 $\overline{\text{OE}}$, 2 $\overline{\text{OE}}$	output enable input (active LOW)
47,46,44,43,41,40,38,37	1A1,1A2,1A3,1A4,1A5,1A6,1A7,1A8	data input or output
36,35,33,32,30,29,27,26	2A1,2A2,2A3,2A4,2A5,2A6,2A7,2A8	data input or output
31,42	V _{CC(A)}	supply voltage A (nAn inputs/outputs, n $\overline{\text{OE}}$ and nDIR inputs are referenced to V _{CC(A)})

Note: All GND pins must be connected to ground (0V).



2.4、Function Table

Supply voltage	Input		Input/output	
$V_{CC(A)}, V_{CC(B)}$	$\overline{nOE}$	nDIR	nAn	nBn
0.8V to 3.6V	L	L	nAn=nBn	input
0.8V to 3.6V	L	H	input	nBn=nAn
0.8V to 3.6V	H	X	Z	Z
GND ^[3]	X	X	Z	Z

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

[2] The nAn, nDIR and $\overline{nOE}$ input circuit is referenced to $V_{CC(A)}$; The nBn input circuit is referenced to $V_{CC(B)}$.

[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	-0.5	+4.6	V
supply voltage B	$V_{CC(B)}$	-	-0.5	+4.6	V
input clamping current	I_{IK}	$V_I < 0V$	-50	-	mA
input voltage	V_I	- ^[1]	-0.5	+4.6	V
output clamping current	I_{OK}	$V_O < 0V$	-50	-	mA
output voltage	V_O	Active mode ^{[1][2][3]}	-0.5	$V_{CCO}+0.5$	V
		Suspend or 3-state mode ^[1]	-0.5	+4.6	V
output current	I_O	$V_O = 0V$ to V_{CCO} ^[2]	-	± 50	mA
supply current	I_{CC}	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
ground current	I_{GND}	-	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	260		°C

Note:

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] $V_{CCO}+0.5V$ should not exceed 4.6V.



3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	0.8	-	3.6	V
supply voltage B	$V_{CC(B)}$	-	0.8	-	3.6	V
input voltage	V_I	-	0	-	3.6	V
output voltage	V_O	Active mode ^[1]	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	3.6	V
ambient temperature	T_{amb}	-	-40	-	+125	°C
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CCI}=0.8V$ to $3.6V$ ^[2]	-	-	5	ns/V

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)^{[1][2]}

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL} $I_O=-1.5mA$; $V_{CC(A)}=V_{CC(B)}=0.8V$	-	0.69	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL} $I_O=1.5mA$; $V_{CC(A)}=V_{CC(B)}=0.8V$	-	0.07	-	V
input leakage current	I_I	nDIR,n OE input; $V_I=0V$ to $3.6V$; $V_{CC(A)}=V_{CC(B)}=0.8V$ to $3.6V$	-	-	± 1	μA
OFF-state output current	I_{OZ}	A or B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=V_{CC(B)}=3.6V$ ^[3]	-	-	± 2.5	μA
		suspend mode A port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$ ^[3]	-	-	± 2.5	μA
		suspend mode B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$ ^[3]	-	-	± 2.5	μA
power-off leakage current	I_{OFF}	A port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(A)}=0V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	± 1	μA
		B port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(B)}=0V$; $V_{CC(A)}=0.8V$ to $3.6V$	-	-	± 1	μA
input capacitance	C_I	nDIR,n OE input; $V_I=0V$ or $3.3V$; $V_{CC(A)}=V_{CC(B)}=3.3V$	-	2.0	-	pF
input/output capacitance	$C_{I/O}$	A and B port; $V_O=3.3V$ or $0V$; $V_{CC(A)}=V_{CC(B)}=3.3V$	-	4.5	-	pF

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.



3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)^{[1][2]}

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	data input	V _{CCI} =0.8V	0.70V _{CCI}	-	V
			V _{CCI} =1.1V to 1.95V	0.65V _{CCI}	-	V
			V _{CCI} =2.3V to 2.7V	1.6	-	V
			V _{CCI} =3.0V to 3.6V	2	-	V
	nDIR, n $\overline{\text{OE}}$ input		V _{CC(A)} =0.8V	0.70V _{CC(A)}	-	V
			V _{CC(A)} =1.1V to 1.95V	0.65V _{CC(A)}	-	V
			V _{CC(A)} =2.3V to 2.7V	1.6	-	V
LOW-level input voltage	V _{IL}	data input	V _{CCI} =0.8V	-	-	0.30V _{CCI}
			V _{CCI} =1.1V to 1.95V	-	-	0.35V _{CCI}
			V _{CCI} =2.3V to 2.7V	-	-	0.7
			V _{CCI} =3.0V to 3.6V	-	-	0.8
	nDIR, n $\overline{\text{OE}}$ input		V _{CC(A)} =0.8V	-	-	0.30V _{CC(A)}
			V _{CC(A)} =1.1V to 1.95V	-	-	0.35V _{CC(A)}
			V _{CC(A)} =2.3V to 2.7V	-	-	0.7
HIGH-level output voltage	V _{OH}	V _I =V _{IH} or V _{IL}	I _O =-100uA; V _{CC(A)} =V _{CC(B)} =0.8V to 3.6V	V _{CCO} -0.1	-	V
			I _O =-3mA; V _{CC(A)} =V _{CC(B)} =1.1V	0.85	-	V
			I _O =-6mA; V _{CC(A)} =V _{CC(B)} =1.4V	1.05	-	V
			I _O =-8mA; V _{CC(A)} =V _{CC(B)} =1.65V	1.2	-	V
			I _O =-9mA; V _{CC(A)} =V _{CC(B)} =2.3V	1.75	-	V
			I _O =-12mA; V _{CC(A)} =V _{CC(B)} =3.0V	2.3	-	V
LOW-level output voltage	V _{OL}	V _I =V _{IH} or V _{IL}	I _O =100uA; V _{CC(A)} =V _{CC(B)} =0.8V to 3.6V	-	-	0.1
			I _O =3mA; V _{CC(A)} =V _{CC(B)} =1.1V	-	-	0.25
			I _O =6mA; V _{CC(A)} =V _{CC(B)} =1.4V	-	-	0.35
			I _O =8mA; V _{CC(A)} =V _{CC(B)} =1.65V	-	-	0.45
			I _O =9mA; V _{CC(A)} =V _{CC(B)} =2.3V	-	-	0.55
			I _O =12mA; V _{CC(A)} =V _{CC(B)} =3.0V	-	-	0.7
input leakage current	I _I	nDIR, n $\overline{\text{OE}}$ input; V _I =0V or 3.6V; V _{CC(A)} =V _{CC(B)} =0.8V to 3.6V	-	-	±1	uA
OFF-state output	I _{OZ}	A or B port; V _O =0V or V _{CCO} ; V _{CC(A)} =V _{CC(B)} =3.6V ^[3]	-	-	±5	uA



current		suspend mode A port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=3.6V$; $V_{CC(B)}=0V^{[3]}$		-	-	± 5	μA
		suspend mode B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=0V$; $V_{CC(B)}=3.6V^{[3]}$		-	-	± 5	μA
power-off leakage current	I_{OFF}	A port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(A)}=0V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	± 5	μA
		B port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(B)}=0V$; $V_{CC(A)}=0.8V$ to $3.6V$		-	-	± 5	μA
supply current	I_{CC}	A port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	30	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	25	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-	-	25	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-5	-	-	μA
		B port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	30	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	25	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-5	-	-	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-	-	25	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ; $V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	55	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ; $V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$		-	-	45	μA

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.



3.3.3、DC Characteristics 3

(T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)^{[1][2]}

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	data input	V _{CCI} =0.8V	0.70V _{CCI}	-	V
			V _{CCI} =1.1V to 1.95V	0.65V _{CCI}	-	V
			V _{CCI} =2.3V to 2.7V	1.6	-	V
			V _{CCI} =3.0V to 3.6V	2	-	V
		nDIR, $\overline{\text{nOE}}$ input	V _{CC(A)} =0.8V	0.70V _{CC(A)}	-	V
			V _{CC(A)} =1.1V to 1.95V	0.65V _{CC(A)}	-	V
			V _{CC(A)} =2.3V to 2.7V	1.6	-	V
LOW-level input voltage	V _{IL}	data input	V _{CCI} =0.8V	-	-	0.30V _{CCI}
			V _{CCI} =1.1V to 1.95V	-	-	0.35V _{CCI}
			V _{CCI} =2.3V to 2.7V	-	-	0.7
			V _{CCI} =3.0V to 3.6V	-	-	0.8
		nDIR, $\overline{\text{nOE}}$ input	V _{CC(A)} =0.8V	-	-	0.30V _{CC(A)}
			V _{CC(A)} =1.1V to 1.95V	-	-	0.35V _{CC(A)}
			V _{CC(A)} =2.3V to 2.7V	-	-	0.7
HIGH-level output voltage	V _{OH}	V _I =V _{IH} or V _{IL}	I _O =-100uA; V _{CC(A)} =V _{CC(B)} =0.8V to 3.6V	V _{CCO} -0.1	-	V
			I _O =-3mA; V _{CC(A)} =V _{CC(B)} =1.1V	0.85	-	V
			I _O =-6mA; V _{CC(A)} =V _{CC(B)} =1.4V	1.05	-	V
			I _O =-8mA; V _{CC(A)} =V _{CC(B)} =1.65V	1.2	-	V
			I _O =-9mA; V _{CC(A)} =V _{CC(B)} =2.3V	1.75	-	V
			I _O =-12mA; V _{CC(A)} =V _{CC(B)} =3.0V	2.3	-	V
LOW-level output voltage	V _{OL}	V _I =V _{IH} or V _{IL}	I _O =100uA; V _{CC(A)} =V _{CC(B)} =0.8V to 3.6V	-	-	0.1
			I _O =3mA; V _{CC(A)} =V _{CC(B)} =1.1V	-	-	0.25
			I _O =6mA; V _{CC(A)} =V _{CC(B)} =1.4V	-	-	0.35
			I _O =8mA; V _{CC(A)} =V _{CC(B)} =1.65V	-	-	0.45
			I _O =9mA; V _{CC(A)} =V _{CC(B)} =2.3V	-	-	0.55
			I _O =12mA; V _{CC(A)} =V _{CC(B)} =3.0V	-	-	0.7
input leakage current	I _I	nDIR, $\overline{\text{nOE}}$ input; V _I =0V or 3.6V; V _{CC(A)} =V _{CC(B)} =0.8V to 3.6V	-	-	±5	uA
OFF-state output	I _{OZ}	A or B port; V _O =0V or V _{CCO} ; V _{CC(A)} =V _{CC(B)} =3.6V ^[3]	-	-	±30	uA



current		suspend mode A port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=3.6V$; $V_{CC(B)}=0V^{[3]}$		-	-	± 30	μA
		suspend mode B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=0V$; $V_{CC(B)}=3.6V^{[3]}$		-	-	± 30	μA
power-off leakage current	I_{OFF}	A port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(A)}=0V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	± 30	μA
		B port; V_I or $V_O=0V$ to $3.6V$; $V_{CC(B)}=0V$; $V_{CC(A)}=0.8V$ to $3.6V$		-	-	± 30	μA
supply current	I_{CC}	A port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	125	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	100	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-	-	100	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-20	-	-	μA
		B port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$	-	-	125	μA
			$V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$	-	-	100	μA
			$V_{CC(A)}=3.6V$; $V_{CC(B)}=0V$	-20	-	-	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=3.6V$	-	-	100	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ; $V_{CC(A)}=0.8V$ to $3.6V$; $V_{CC(B)}=0.8V$ to $3.6V$		-	-	185	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI} ; $V_{CC(A)}=1.1V$ to $3.6V$; $V_{CC(B)}=1.1V$ to $3.6V$		-	-	150	μA

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

3.3.4、Typical total supply current ($I_{CC(A)}+I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0V	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
0V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA



3.3.5、AC Characteristics 1

($V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
power dissipation capacitance	C_{PD}	A port: (direction A to B); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction A to B); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction B to A); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		A port: (direction B to A); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction A to B); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		B port: (direction A to B); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction B to A); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction B to A); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

Note:

C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =load capacitance in pF;

V_{CC} =supply voltage in V;

N =number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of the outputs.

$f_i=10\text{MHz}$; $V_I=\text{GND to } V_{CC}$; $t_r=t_f=1\text{ns}$; $C_L=0\text{pF}$; $R_L=\infty\Omega$.



3.3.6、AC Characteristics 2

($V_{CC(A)}=0.8V$ and $T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(A)}=V_{CC(B)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
propagation delay	t_{pd}	nAn to nBn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		nBn to nAn	14.4	12.4	12.1	11.9	11.8	11.8	ns
disable time	t_{dis}	$\overline{nOE}$ to nAn	16.2	16.2	16.2	16.2	16.2	16.2	ns
		$\overline{nOE}$ to nBn	17.6	10.0	9.0	9.1	8.7	9.3	ns
enable time	t_{en}	$\overline{nOE}$ to nAn	21.9	21.9	21.9	21.9	21.9	21.9	ns
		$\overline{nOE}$ to nBn	22.2	11.1	9.8	9.4	9.4	9.6	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

3.3.7、AC Characteristics 3

($V_{CC(B)}=0.8V$ and $T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(A)}=V_{CC(B)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
propagation delay	t_{pd}	nAn to nBn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		nBn to nAn	14.4	7.0	6.2	6.0	5.9	6.0	ns
disable time	t_{dis}	$\overline{nOE}$ to nAn	16.2	5.9	4.4	4.2	3.1	3.5	ns
		$\overline{nOE}$ to nBn	17.6	14.2	13.7	13.6	13.3	13.1	ns
enable time	t_{en}	$\overline{nOE}$ to nAn	21.9	6.4	4.4	3.5	2.6	2.3	ns
		$\overline{nOE}$ to nBn	22.2	17.7	17.2	17.0	16.8	16.7	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .



3.3.8、DC Characteristics 4

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	V _{CC(B)}										Unit
			1.2V ±0.1V		1.5V ±0.1V		1.8V ±0.15V		2.5V ±0.2V		3.3V ±0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{CC(A)} =1.1V to 1.3V													
propagation delay	t _{pd}	nAn to nBn	0.5	9.2	0.5	6.9	0.5	6.0	0.5	5.1	0.5	4.9	ns
		nBn to nAn	0.5	9.2	0.5	8.7	0.5	8.5	0.5	8.2	0.5	8.0	ns
disable time	t _{dis}	n $\overline{\text{OE}}$ to nAn	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.5	1.5	9.7	1.5	9.5	1.0	8.1	1.0	8.9	ns
enable time	t _{en}	n $\overline{\text{OE}}$ to nAn	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	ns
		n $\overline{\text{OE}}$ to nBn	1.1	14.9	1.1	11.0	1.1	9.6	1.0	8.1	1.0	7.7	ns
V _{CC(A)} =1.4V to 1.6V													
propagation delay	t _{pd}	nAn to nBn	0.5	8.7	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns
		nBn to nAn	0.5	6.9	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns
disable time	t _{dis}	n $\overline{\text{OE}}$ to nAn	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.4	1.5	8.7	1.5	7.5	1.0	6.5	1.0	6.3	ns
enable time	t _{en}	n $\overline{\text{OE}}$ to nAn	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	ns
		n $\overline{\text{OE}}$ to nBn	1.0	13.5	1.0	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns
V _{CC(A)} =1.65V to 1.95V													
propagation delay	t _{pd}	nAn to nBn	0.5	8.5	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns
		nBn to nAn	0.5	6.0	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns
disable time	t _{dis}	n $\overline{\text{OE}}$ to nAn	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.1	1.5	8.4	1.5	7.1	1.0	5.9	1.0	5.7	ns
enable time	t _{en}	n $\overline{\text{OE}}$ to nAn	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns
		n $\overline{\text{OE}}$ to nBn	1.0	13.0	1.0	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns
V _{CC(A)} =2.3V to 2.7V													
propagation delay	t _{pd}	nAn to nBn	0.5	8.2	0.5	5.6	0.5	4.6	0.5	3.3	0.5	2.8	ns
		nBn to nAn	0.5	5.1	0.5	4.1	0.5	3.7	0.5	3.4	0.5	3.2	ns
disable time	t _{dis}	n $\overline{\text{OE}}$ to nAn	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	ns
		n $\overline{\text{OE}}$ to nBn	1.0	10.6	1.0	7.9	1.0	6.6	1.0	6.1	1.0	5.2	ns
enable time	t _{en}	n $\overline{\text{OE}}$ to nAn	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
		n $\overline{\text{OE}}$ to nBn	0.5	12.5	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns
V _{CC(A)} =3.0V to 3.6V													
propagation delay	t _{pd}	nAn to nBn	0.5	8.0	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns
		nBn to nAn	0.5	4.9	0.5	3.7	0.5	3.3	0.5	2.9	0.5	2.7	ns
disable time	t _{dis}	n $\overline{\text{OE}}$ to nAn	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	ns
		n $\overline{\text{OE}}$ to nBn	1.0	10.3	1.0	7.7	1.0	6.5	1.0	5.2	0.5	5.0	ns
enable time	t _{en}	n $\overline{\text{OE}}$ to nAn	0.5	4.3	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4.0	ns
		n $\overline{\text{OE}}$ to nBn	0.5	12.4	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4.0	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .



3.3.9、DC Characteristics 5

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

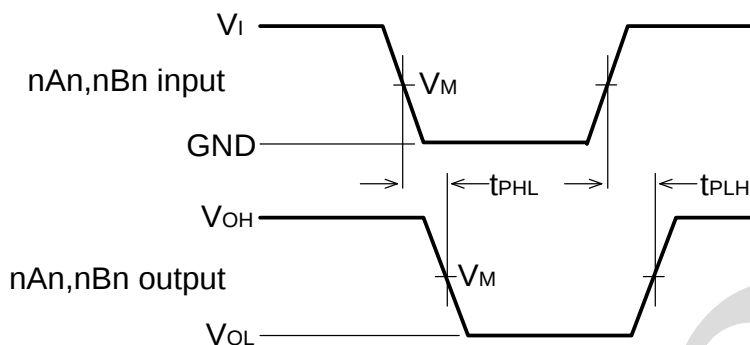
Parameter	Symbol	Conditions	V _{CC(B)}										Unit
			1.2V ±0.1V		1.5V ±0.1V		1.8V ±0.15V		2.5V ±0.2V		3.3V ±0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{CC(A)} =1.1V to 1.3V													
propagation delay	t _{pd}	nAn to nBn	0.5	10.2	0.5	7.6	0.5	6.6	0.5	5.7	0.5	5.4	ns
		nBn to nAn	0.5	10.2	0.5	9.6	0.5	9.4	0.5	9.1	0.5	8.8	ns
disable time	t _{dis}	n $\overline{OE}$ to nAn	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	ns
		n $\overline{OE}$ to nBn	1.5	13.8	1.5	10.7	1.5	10.5	1.0	9.0	1.0	9.8	ns
enable time	t _{en}	n $\overline{OE}$ to nAn	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	ns
		n $\overline{OE}$ to nBn	1.1	16.4	1.1	12.1	1.1	10.6	1.0	9.0	1.0	8.5	ns
V _{CC(A)} =1.4V to 1.6V													
propagation delay	t _{pd}	nAn to nBn	0.5	9.6	0.5	6.9	0.5	5.8	0.5	4.6	0.5	4.1	ns
		nBn to nAn	0.5	7.6	0.5	6.9	0.5	6.5	0.5	6.2	0.5	6.1	ns
disable time	t _{dis}	n $\overline{OE}$ to nAn	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	ns
		n $\overline{OE}$ to nBn	1.5	12.6	1.5	9.6	1.5	8.3	1.0	7.2	1.0	7.0	ns
enable time	t _{en}	n $\overline{OE}$ to nAn	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	ns
		n $\overline{OE}$ to nBn	1.0	14.9	1.0	11.2	0.5	9.0	0.5	6.5	0.5	5.8	ns
V _{CC(A)} =1.65V to 1.95V													
propagation delay	t _{pd}	nAn to nBn	0.5	9.4	0.5	6.5	0.5	5.3	0.5	4.1	0.5	3.7	ns
		nBn to nAn	0.5	6.6	0.5	5.8	0.5	5.3	0.5	5.0	0.5	4.9	ns
disable time	t _{dis}	n $\overline{OE}$ to nAn	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns
		n $\overline{OE}$ to nBn	1.5	12.3	1.5	9.3	1.5	7.9	1.0	6.5	1.0	6.3	ns
enable time	t _{en}	n $\overline{OE}$ to nAn	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	ns
		n $\overline{OE}$ to nBn	1.0	14.3	1.0	10.2	0.5	8.2	0.5	5.9	0.5	5.0	ns
V _{CC(A)} =2.3V to 2.7V													
propagation delay	t _{pd}	nAn to nBn	0.5	9.1	0.5	6.2	0.5	5.1	0.5	3.7	0.5	3.1	ns
		nBn to nAn	0.5	5.7	0.5	4.6	0.5	4.1	0.5	3.8	0.5	3.6	ns
disable time	t _{dis}	n $\overline{OE}$ to nAn	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	ns
		n $\overline{OE}$ to nBn	1.0	11.7	1.0	8.7	1.0	7.3	1.0	6.8	1.0	5.8	ns
enable time	t _{en}	n $\overline{OE}$ to nAn	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	ns
		n $\overline{OE}$ to nBn	0.5	13.8	0.5	10.4	0.5	8.1	0.5	5.7	0.5	5.0	ns
V _{CC(A)} =3.0V to 3.6V													
propagation delay	t _{pd}	nAn to nBn	0.5	8.8	0.5	6.1	0.5	4.9	0.5	3.6	0.5	3.0	ns
		nBn to nAn	0.5	5.4	0.5	4.1	0.5	3.7	0.5	3.2	0.5	3.0	ns
disable time	t _{dis}	n $\overline{OE}$ to nAn	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	ns
		n $\overline{OE}$ to nBn	1.0	11.4	1.0	8.5	1.0	7.2	1.0	5.8	0.5	5.5	ns
enable time	t _{en}	n $\overline{OE}$ to nAn	0.5	4.8	0.5	4.8	0.5	4.7	0.5	4.6	0.5	4.4	ns
		n $\overline{OE}$ to nBn	0.5	13.7	0.5	10.3	0.5	8.0	0.5	5.4	0.5	4.4	ns

Note: t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

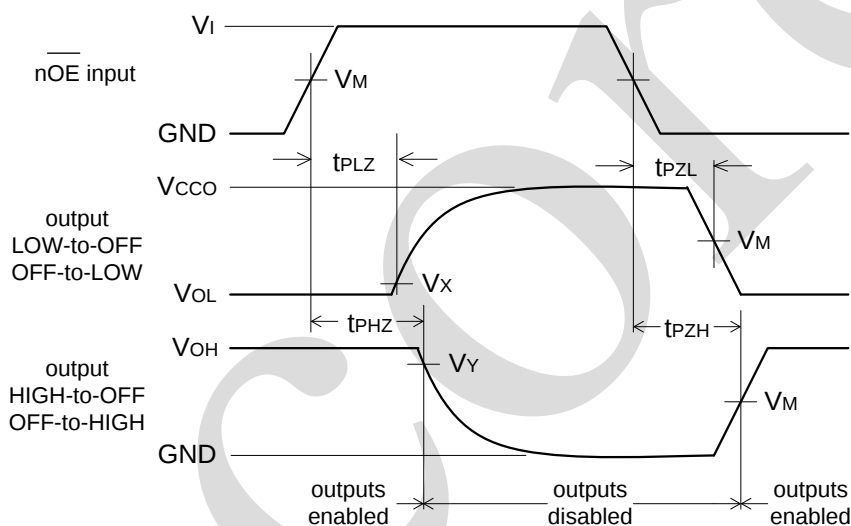


4、Testing Circuit

4.1、AC Testing Waveforms



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
Figure 3. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
Figure 4. Enable and disable times

4.2、Measurement Points

Supply voltage	Input ^[1]	Output ^[2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.1V$	$V_{OH}-0.1V$
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.15V$	$V_{OH}-0.15V$
3.0V to 3.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.3V$	$V_{OH}-0.3V$

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.



4.3、AC Testing Circuit

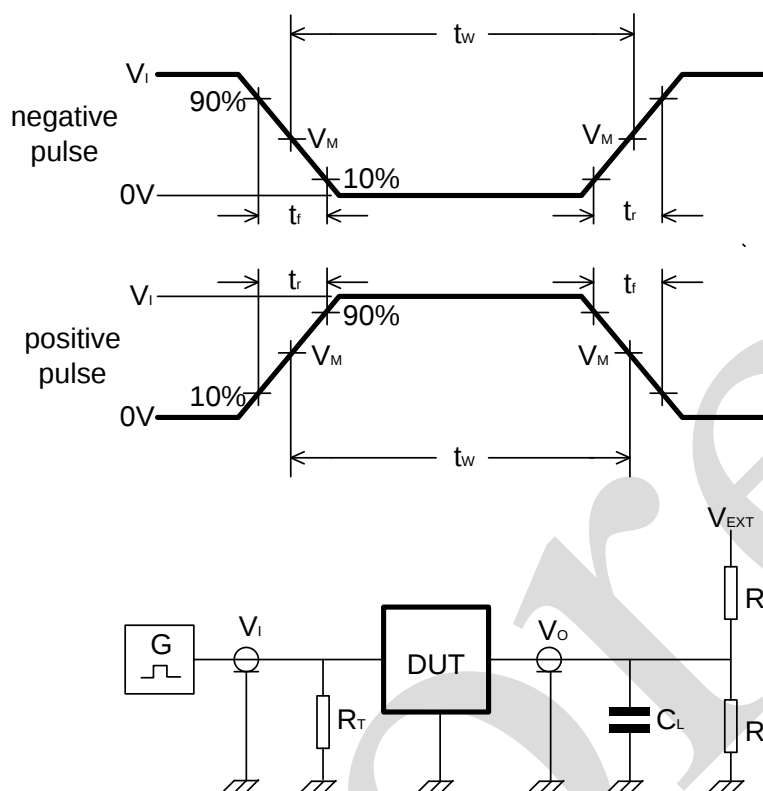


Figure 5. Load circuitry for switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance.

V_{EXT} =External voltage for measuring switching times.

4.4、Test Data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	$V_I^{[1]}$	$\Delta t/\Delta V^{[2]}$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	$t_{PZL}, t_{PLZ}^{[3]}$
0.8V to 1.6V	V_{CCI}	$\leq 1.0\text{ns/V}$	15pF	2k Ω	open	GND	2V $_{CCO}$
1.65V to 2.7V	V_{CCI}	$\leq 1.0\text{ns/V}$	15pF	2k Ω	open	GND	2V $_{CCO}$
3.0V to 3.6V	V_{CCI}	$\leq 1.0\text{ns/V}$	15pF	2k Ω	open	GND	2V $_{CCO}$

Note:

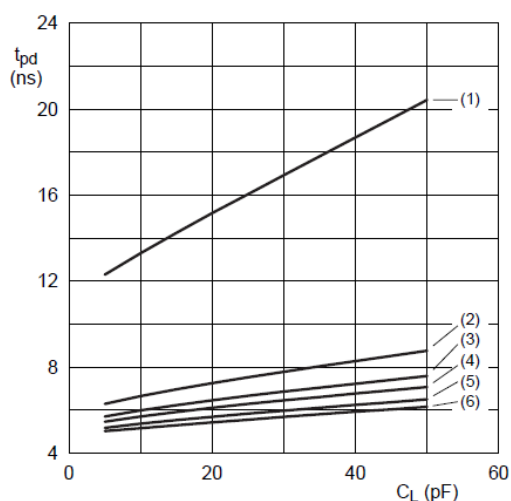
[1] V_{CCI} is the supply voltage associated with the data input port.

[2] $dV/dt \geq 1.0\text{V/ns}$.

[3] V_{CCO} is the supply voltage associated with the output port.

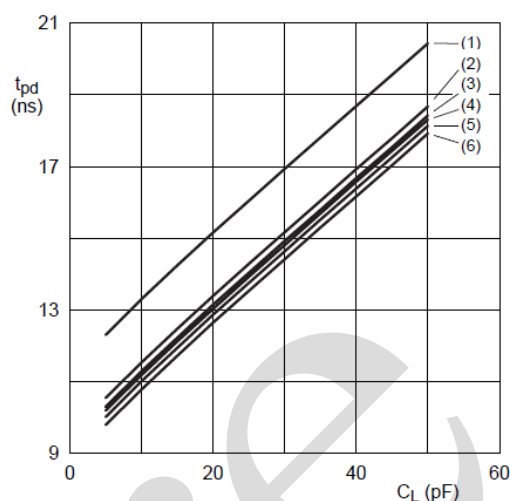


5、Characteristic Curve



a. Propagation delay (A to B); $V_{CC(A)}=0.8V$

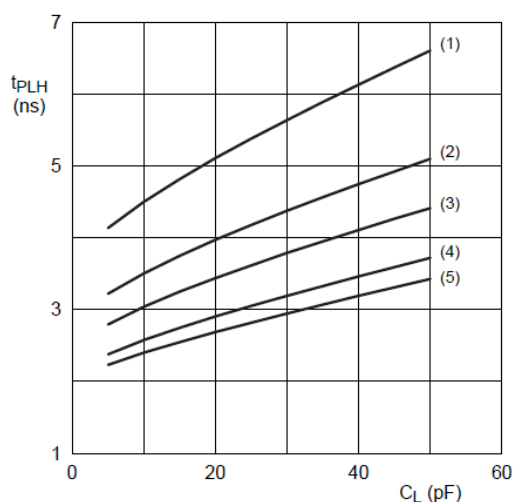
- (1) $V_{CC(B)}=0.8V$.
- (2) $V_{CC(B)}=1.2V$.
- (3) $V_{CC(B)}=1.5V$.
- (4) $V_{CC(B)}=1.8V$.
- (5) $V_{CC(B)}=2.5V$.
- (6) $V_{CC(B)}=3.3V$.



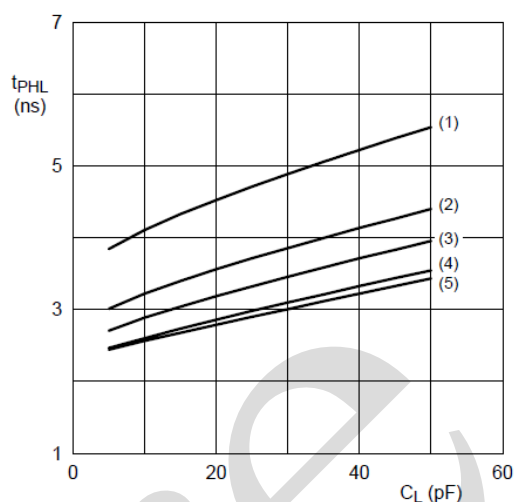
b. Propagation delay (A to B); $V_{CC(B)}=0.8V$

- (1) $V_{CC(A)}=0.8V$.
- (2) $V_{CC(A)}=1.2V$.
- (3) $V_{CC(A)}=1.5V$.
- (4) $V_{CC(A)}=1.8V$.
- (5) $V_{CC(A)}=2.5V$.
- (6) $V_{CC(A)}=3.3V$.

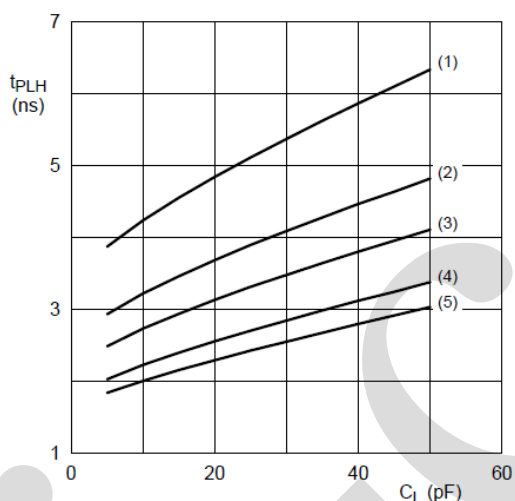
Figure 6. Typical propagation delay vs load capacitance; $T_{amb}=25^{\circ}C$



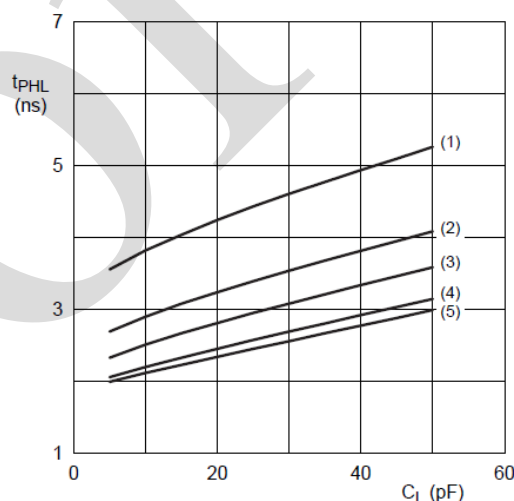
a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.2V$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.2V$



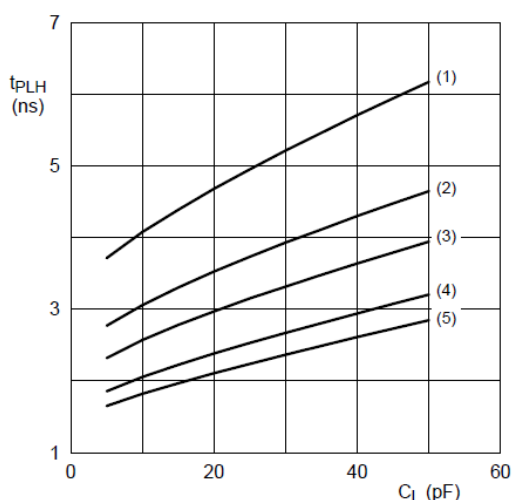
c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.5V$



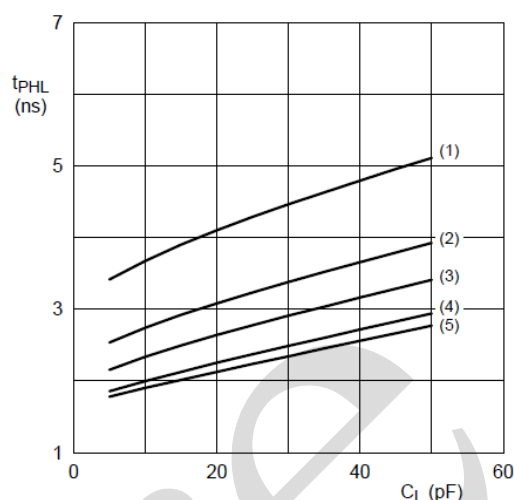
d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.5V$

- (1) $V_{CC(B)}=1.2V$.
- (2) $V_{CC(B)}=1.5V$.
- (3) $V_{CC(B)}=1.8V$.
- (4) $V_{CC(B)}=2.5V$.
- (5) $V_{CC(B)}=3.3V$.

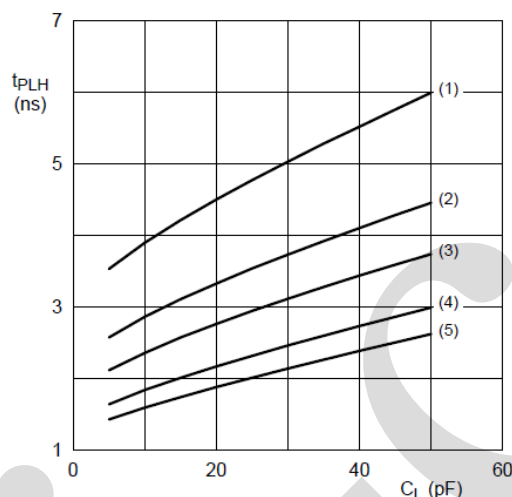
Figure 7. Typical propagation delay vs load capacitance; $T_{amb}=25^{\circ}C$



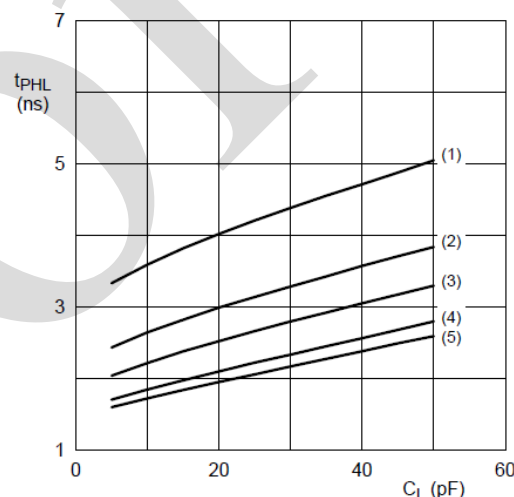
a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.8V$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.8V$



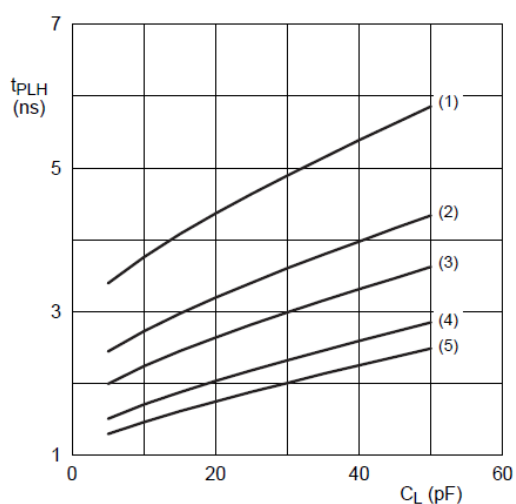
c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=2.5V$



d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=2.5V$

- (1) $V_{CC(B)}=1.2V$.
- (2) $V_{CC(B)}=1.5V$.
- (3) $V_{CC(B)}=1.8V$.
- (4) $V_{CC(B)}=2.5V$.
- (5) $V_{CC(B)}=3.3V$.

Figure 8. Typical propagation delay vs load capacitance; $T_{amb}=25^{\circ}C$



a. LOW to HIGH propagation delay (A to B);

$V_{CC(A)}=3.3V$

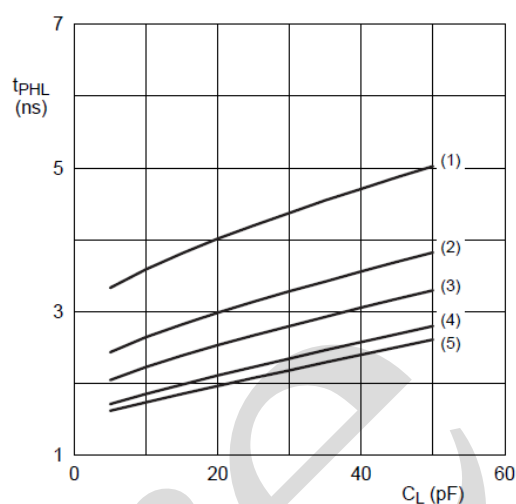
(1) $V_{CC(B)}=1.2V$.

(2) $V_{CC(B)}=1.5V$.

(3) $V_{CC(B)}=1.8V$.

(4) $V_{CC(B)}=2.5V$.

(5) $V_{CC(B)}=3.3V$.



b. HIGH to LOW propagation delay (A to B);

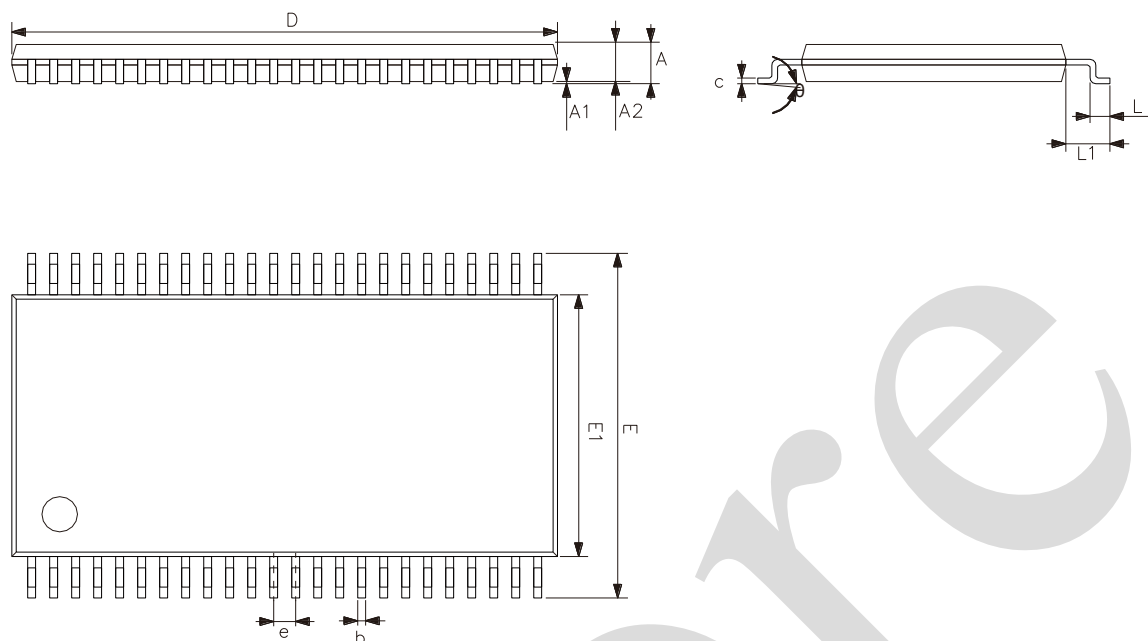
$V_{CC(A)}=3.3V$

Figure 9. Typical propagation delay vs load capacitance; $T_{amb}=25^{\circ}C$



6、Package Information

6.1、TSSOP48



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.03	0.15
A2	0.82	1.05
b	0.17	0.27
c	0.12	0.22
D	12.40	12.60
E	7.90	8.30
E1	6.00	6.20
e	0.50	
L	0.35	0.75
L1	1.00	
θ	0°	8°



7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We Recommend you to read this chapter carefully before using this product.

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