# AiP74AVCH2T45
# 2-bit Dual Supply Translating Transceiver;3-state

# Product Specification

**Specification Revision History：**

| Version | Date | Description |
|---|---|---|
| 2019-04-A1 | 2019-04 | New |
| 2023-04-B1 | 2023-04 | Update the template |
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# Contents

## 1、General Description

The AiP74AVCH2T45 is a dual bit, dual supply transceiver that enables bidirectional level translation. It features two data input-output ports (nA and nB), a direction control input(DIR) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8V and 3.6V making the device suitable for translating between any of the low voltage nodes (0.8V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V). Pins nA and DIR are referenced to $V_{CC(A)}$ and pins nB are referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from nA to nB and a LOW on DIR allows transmission from nB to nA.

The device is fully specified for partial power-down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A and B are in the high-impedance OFF-state.

The AiP74AVCH2T45 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

**Features:**

- Wide supply voltage range:
  $V_{CC(A)}$: 0.8V to 3.6V
  $V_{CC(B)}$: 0.8V to 3.6V
- Maximum data rates:
  500Mbps (1.8V to 3.3V translation)
  320Mbps (<1.8V to 3.3V translation)
  320Mbps (translate to 2.5V or 1.8V)
  280Mbps (translate to 1.5V)
  240Mbps (translate to 1.2V)
- Suspend mode
- Bus hold on data inputs
- Inputs accept voltages up to 3.6V
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- Specified from -40℃ to +125℃
- Packaging information: TSSOP8/VSSOP8

**Ordering Information:**

**Tube packing specifications:**

| Part number | Packaging form | Marking code | Tube quantity | Boxed tube quantity | Boxed quantity | Notes |
|---|---|---|---|---|---|---|
| AiP74AVCH2T45TA8.TB | TSSOP8 | CGXX | 100 PCS/tube | 200 tube/box | 20000 PCS/box | Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm |

**Reel packing specifications:**

| Part number | Packaging form | Marking code | Reel quantity | Boxed reel quantity | Notes |
|---|---|---|---|---|---|
| AiP74AVCH2T45TA8.TR | TSSOP8 | CGXX | 3000 PCS/reel | 3000 PCS/box | Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing:0.65mm |
| AiP74AVCH2T45YA8.TR | VSSOP8 | CGXX | 3000 PCS/reel | 3000 PCS/box | Dimensions of plastic enclosure: 2.0mm×2.3mm Pin spacing:0.50mm |

Note 1: "XX" refers to variable content, meaning year and package batch serial number.

Note 2: If the physical information is inconsistent with the ordering information, please refer to the actual product.

## 2、Block Diagram And Pin Description

### 2.1、Block Diagram

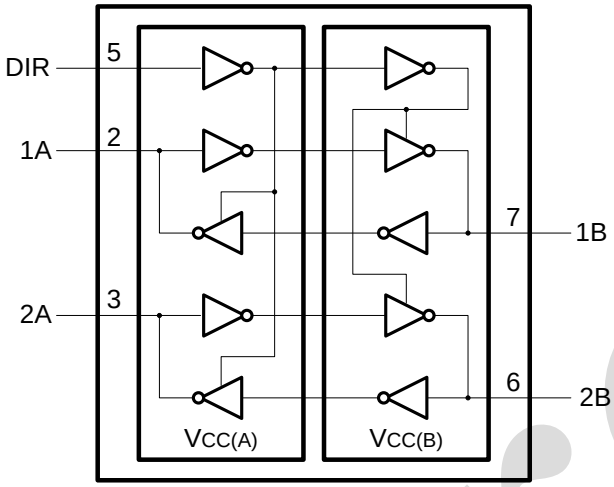



Figure 1. Logic symbol

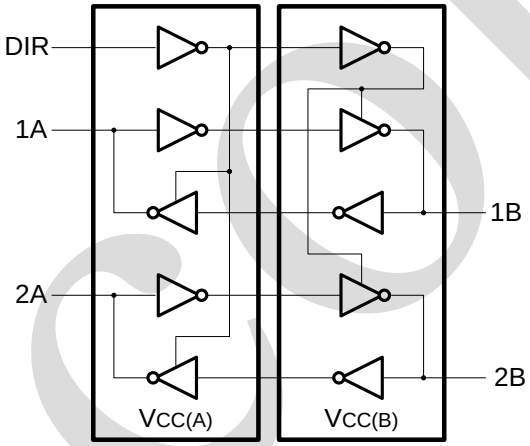
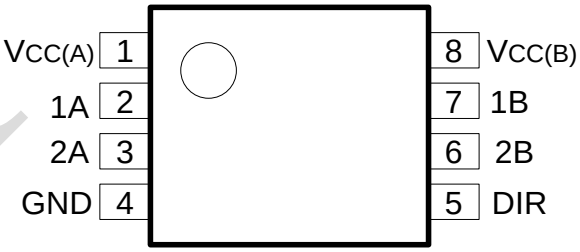



Figure 2. Logic diagram

### 2.2、Pin Configurations



### 2.3、Pin Description

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | $V_{CC(A)}$ | supply voltage port A and DIR |
| 2 | 1A | data input or output |
| 3 | 2A | data input or output |
| 4 | GND | ground (0 V) |
| 5 | DIR | direction control |
| 6 | 2B | data input or output |
| 7 | 1B | data input or output |
| 8 | $V_{CC(B)}$ | supply voltage port B |

### 2.4、Function Table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

| Supply voltage | Input | Input/output[1] | |
|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | DIR[2] | nA | nB |
| 0.8V to 3.6V | L | nA=nB | input |
| 0.8V to 3.6V | H | input | nB=nA |
| GND[3] | X | Z | Z |

Note:

[1] The input circuit of the data I/O is always active.

[2] The DIR input circuit is referenced to $V_{CC(A)}$.

[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

## 3、Electrical Parameter

### 3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Characteristic | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage A | $V_{CC(A)}$ | - | -0.5 | +4.6 | V |
| Supply Voltage B | $V_{CC(B)}$ | - | -0.5 | +4.6 | V |
| input clamping current | $I_{IK}$ | $V_I$<0V | -50 | - | mA |
| Input Voltage | $V_I$ | -[1] | -0.5 | +4.6 | V |
| output clamping current | $I_{OK}$ | $V_O$<0V | -50 | - | mA |
| output voltage | $V_O$ | Active mode[1][2][3] | -0.5 | $V_{CCO}$ +0.5 | V |
| | | Suspend or 3-state mode[1] | -0.5 | +4.6 | V |
| output current | $I_O$ | $V_O$=0V to $V_{CCO}$ | - | ±50 | mA |
| supply current | $I_{CC}$ | $I_{CC(A)}$ or $I_{CC(B)}$ | - | 100 | mA |
| ground current | $I_{GND}$ | - | -100 | - | mA |
| Storage Temperature | $T_{stg}$ | - | -65 | +150 | ℃ |
| total power dissipation | $P_{tot}$ | - | - | 250 | mW |
| Soldering Temperature | $T_L$ | 10s | 260 | | ℃ |

Note:

[1] The minimum input voltage rating and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] $V_{CCO}$ is the supply voltage associated with the output port.

[3] $V_{CCO}$+0.5V should not exceed 4.6V.

### 3.2、Recommended Operating Conditions

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| supply voltage A | $V_{CC(A)}$ | - | 0.8 | - | 3.6 | V |
| supply voltage B | $V_{CC(B)}$ | - | 0.8 | - | 3.6 | V |
| input voltage | $V_I$ | - | 0 | - | 3.6 | V |
| output voltage | $V_O$ | Active mode[1] | 0 | - | $V_{CCO}$ | V |
| | | Suspend or 3-state mode | 0 | - | 3.6 | V |
| ambient temperature | $T_{amb}$ | - | -40 | - | +125 | ℃ |
| input transition rise and fall rate | Δt/ΔV | $V_{CCI}$=0.8V to 3.6V | - | - | 5 | ns/V |

Note:

[1] $V_{CCO}$ is the supply voltage associated with the output port.

### 3.3、Electrical Characteristics

#### 3.3.1、DC Characteristics 1

($T_{amb}$=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified)[1][2]

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level output voltage | $V_{OH}$ | $V_I$=$V_{IH}$ or $V_{IL}$ | $I_O$=-1.5mA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V | - | 0.69 | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$=$V_{IH}$ or $V_{IL}$ | $I_O$=1.5mA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V | - | 0.07 | - | V |
| input leakage current | $I_I$ | DIR input; $V_I$=0V or 3.6V; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V | | - | - | ±1 | uA |
| bus hold LOW current | $I_{BHL}$ | $V_I$=0.42V; $V_{CC(A)}$=$V_{CC(B)}$=1.2V[3] | | - | 26 | - | uA |
| bus hold HIGH current | $I_{BHH}$ | $V_I$=0.78V; $V_{CC(A)}$=$V_{CC(B)}$=1.2V[4] | | - | -24 | - | uA |
| bus hold LOW overdrive current | $I_{BHLO}$ | $V_I$=GND to $V_{CCI}$; $V_{CC(A)}$=$V_{CC(B)}$=1.2V[5] | | - | 28 | - | uA |
| bus hold HIGH overdrive current | $I_{BHHO}$ | $V_I$= GND to $V_{CCI}$; $V_{CC(A)}$=$V_{CC(B)}$=1.2V[6] | | - | -26 | - | uA |
| OFF-state output current | $I_{OZ}$ | A or B port; $V_O$=0V or $V_{CCO}$; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V[7] | | - | - | ±2.5 | uA |
| power-off current leakage | $I_{OFF}$ | A port; $V_I$ or $V_O$=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0.8V to 3.6V | | - | - | ±1 | uA |
| | | B port; $V_I$ or $V_O$=0V to 3.6V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0.8V to 3.6V | | - | - | ±1 | uA |
| input capacitance | $C_I$ | DIR input; $V_I$=0V or 3.3V; $V_{CC(A)}$=$V_{CC(B)}$=3.3V | | - | 1.0 | - | pF |
| input/output capacitance | $C_{I/O}$ | A and B port; Suspend mode; $V_O$=$V_{CCO}$ or GND; $V_{CC(A)}$=$V_{CC(B)}$=3.3V | | - | 4.0 | - | pF |

Note:

[1] $V_{CCO}$ is the supply voltage associated with the output port.

[2] $V_{CCI}$ is the supply voltage associated with the data input port.

[3] The bus hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max.
$I_{BHL}$ should be measured after lowering $V_I$ to GND and then raising it to $V_{IL}$ max.
[4] The bus hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min.
$I_{BHH}$ should be measured after raising $V_I$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.
[5] An external driver must source at least $I_{BHLO}$ to switch this node from LOW to HIGH.
[6] An external driver must sink at least $I_{BHHO}$ to switch this node from HIGH to LOW.
[7] For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

### 3.3.2、DC Characteristics 2

($T_{amb}$=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified)[1][2]

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level input voltage | $V_{IH}$ | data input | $V_{CCI}$=0.8V | 0.70$V_{CCI}$ | - | - | V |
| | | | $V_{CCI}$=1.1V to 1.95V | 0.65$V_{CCI}$ | - | - | V |
| | | | $V_{CCI}$=2.3V to 2.7V | 1.6 | - | - | V |
| | | | $V_{CCI}$=3.0V to 3.6V | 2 | - | - | V |
| | | DIR input | $V_{CC(A)}$=0.8V | 0.70$V_{CC(A)}$ | - | - | V |
| | | | $V_{CC(A)}$=1.1V to 1.95V | 0.65$V_{CC(A)}$ | - | - | V |
| | | | $V_{CC(A)}$=2.3V to 2.7V | 1.6 | - | - | V |
| | | | $V_{CC(A)}$=3.0V to 3.6V | 2 | - | - | V |
| LOW-level input voltage | $V_{IL}$ | data input | $V_{CCI}$=0.8V | - | - | 0.30$V_{CCI}$ | V |
| | | | $V_{CCI}$=1.1V to 1.95V | - | - | 0.35$V_{CCI}$ | V |
| | | | $V_{CCI}$=2.3V to 2.7V | - | - | 0.7 | V |
| | | | $V_{CCI}$=3.0V to 3.6V | - | - | 0.9 | V |
| | | DIR input | $V_{CC(A)}$=0.8V | - | - | 0.30$V_{CC(A)}$ | V |
| | | | $V_{CC(A)}$=1.1V to 1.95V | - | - | 0.35$V_{CC(A)}$ | V |
| | | | $V_{CC(A)}$=2.3V to 2.7V | - | - | 0.7 | V |
| | | | $V_{CC(A)}$=3.0V to 3.6V | - | - | 0.9 | V |
| HIGH-level output voltage | $V_{OH}$ | $V_I$=$V_{IH}$ or $V_{IL}$ | $I_O$=-100uA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V | $V_{CCO}$-0.1 | - | - | V |
| | | | $I_O$=-3mA; $V_{CC(A)}$=$V_{CC(B)}$=1.1V | 0.85 | - | - | V |
| | | | $I_O$=-6mA; $V_{CC(A)}$=$V_{CC(B)}$=1.4V | 1.05 | - | - | V |
| | | | $I_O$=-8 mA; $V_{CC(A)}$=$V_{CC(B)}$=1.65V | 1.2 | - | - | V |
| | | | $I_O$=-9mA; $V_{CC(A)}$=$V_{CC(B)}$=2.3V | 1.75 | - | - | V |
| | | | $I_O$=-12mA; $V_{CC(A)}$=$V_{CC(B)}$=3.0V | 2.3 | - | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$=$V_{IH}$ or $V_{IL}$ | $I_O$=100uA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V | - | - | 0.1 | V |
| | | | $I_O$=3mA; $V_{CC(A)}$=$V_{CC(B)}$=1.1V | - | - | 0.25 | V |
| | | | $I_O$=6mA; $V_{CC(A)}$=$V_{CC(B)}$=1.4V | - | - | 0.35 | V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | $I_O$=8mA; $V_{CC(A)}$=$V_{CC(B)}$=1.65V | - | - | 0.45 | V |
| | | | $I_O$=9mA; $V_{CC(A)}$=$V_{CC(B)}$=2.3V | - | - | 0.55 | V |
| | | | $I_O$=12mA; $V_{CC(A)}$=$V_{CC(B)}$=3.0V | - | - | 0.7 | V |
| input leakage current | $I_I$ | DIR input; $V_I$=0V or 3.6V; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V | | - | - | ±1 | uA |
| bus hold LOW current | $I_{BHL}$ | A or B port[3] | $V_I$=0.49V; $V_{CC(A)}$=$V_{CC(B)}$=1.4V | 15 | - | - | uA |
| | | | $V_I$=0.58V; $V_{CC(A)}$=$V_{CC(B)}$=1.65V | 25 | - | - | uA |
| | | | $V_I$=0.70V; $V_{CC(A)}$=$V_{CC(B)}$=2.3V | 45 | - | - | uA |
| | | | $V_I$=0.80V; $V_{CC(A)}$=$V_{CC(B)}$=3.0V | 100 | - | - | uA |
| bus hold HIGH current | $I_{BHH}$ | A or B port[4] | $V_I$=0.91V; $V_{CC(A)}$=$V_{CC(B)}$=1.4V | -15 | - | - | uA |
| | | | $V_I$=1.07V; $V_{CC(A)}$=$V_{CC(B)}$=1.65V | -25 | - | - | uA |
| | | | $V_I$=1.60V; $V_{CC(A)}$=$V_{CC(B)}$=2.3V | -45 | - | - | uA |
| | | | $V_I$=2.00V; $V_{CC(A)}$=$V_{CC(B)}$=3.0V | -100 | - | - | uA |
| bus hold LOW overdrive current | $I_{BHLO}$ | A or B port[5] | $V_{CC(A)}$=$V_{CC(B)}$=1.6V | 125 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=1.95V | 200 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=2.7V | 300 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=3.6V | 500 | - | - | uA |
| bus hold HIGH overdrive current | $I_{BHHO}$ | A or B port[6] | $V_{CC(A)}$=$V_{CC(B)}$=1.6V | -125 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=1.95V | -200 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=2.7V | -300 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=3.6V | -500 | - | - | uA |
| OFF-state output current | $I_{OZ}$ | A or B port; $V_O$=0V or $V_{CCO}$; $V_{CC(A)}$=$V_{CC(B)}$=0.8 to 3.6V[7] | | - | - | ±5 | uA |
| power-off leakage current | $I_{OFF}$ | A port; $V_I$ or $V_O$=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0.8V to 3.6V | | - | - | ±5 | uA |
| | | B port; $V_I$ or $V_O$=0V to 3.6V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0.8V to 3.6V | | - | - | ±5 | uA |
| supply current | $I_{CC}$ | A port; $V_I$=0V or $V_{CCI}$; $I_O$=0A | $V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V | - | - | 8 | uA |
| | | | $V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V | - | - | 8 | uA |
| | | | $V_{CC(A)}$=0V; $V_{CC(B)}$=3.6V | -2 | - | - | uA |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | B port; $V_I$=0V or $V_{CCI}$; $I_O$=0A | $V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V | - | - | 8 | uA |
| | | | $V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V | -2 | - | - | uA |
| | | | $V_{CC(A)}$=0V; $V_{CC(B)}$=3.6V | - | - | 8 | uA |
| | | A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); $I_O$=0A;$V_I$=0V or $V_{CCI}$; $V_{CC(A)}$=0.8V to 3.6V;$V_{CC(B)}$=0.8V to 3.6V | | - | - | 16 | uA |

Note:

[1] $V_{CCO}$ is the supply voltage associated with the output port.

[2] $V_{CCI}$ is the supply voltage associated with the data input port.

[3] The bus hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max. $I_{BHL}$ should be measured after lowering $V_I$ to GND and then raising it to $V_{IL}$ max.

[4] The bus hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min. $I_{BHH}$ should be measured after raising $V_I$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.

[5] An external driver must source at least $I_{BHLO}$ to switch this node from LOW to HIGH.

[6] An external driver must sink at least $I_{BHHO}$ to switch this node from HIGH to LOW.

[7] For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

### 3.3.3、DC Characteristics 3

($T_{amb}$=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified)[1][2]

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level input voltage | $V_{IH}$ | data input | $V_{CCI}$=0.8V | 0.70$V_{CCI}$ | - | - | V |
| | | | $V_{CCI}$=1.1V to 1.95V | 0.65$V_{CCI}$ | - | - | V |
| | | | $V_{CCI}$=2.3V to 2.7V | 1.6 | - | - | V |
| | | | $V_{CCI}$=3.0V to 3.6V | 2 | - | - | V |
| | | DIR input | $V_{CC(A)}$=0.8V | 0.70$V_{CC(A)}$ | - | - | V |
| | | | $V_{CC(A)}$=1.1V to 1.95V | 0.65$V_{CC(A)}$ | - | - | V |
| | | | $V_{CC(A)}$=2.3V to 2.7V | 1.6 | - | - | V |
| | | | $V_{CC(A)}$=3.0V to 3.6V | 2 | - | - | V |
| LOW-level input voltage | $V_{IL}$ | data input | $V_{CCI}$=0.8V | - | - | 0.30$V_{CCI}$ | V |
| | | | $V_{CCI}$=1.1V to 1.95V | - | - | 0.35$V_{CCI}$ | V |
| | | | $V_{CCI}$=2.3V to 2.7V | - | - | 0.7 | V |
| | | | $V_{CCI}$=3.0V to 3.6V | - | - | 0.9 | V |
| | | DIR input | $V_{CC(A)}$=0.8V | - | - | 0.30$V_{CC(A)}$ | V |
| | | | $V_{CC(A)}$=1.1V to 1.95V | - | - | 0.35$V_{CC(A)}$ | V |
| | | | $V_{CC(A)}$=2.3V to 2.7V | - | - | 0.7 | V |
| | | | $V_{CC(A)}$=3.0V to 3.6V | - | - | 0.9 | V |
| HIGH-level output voltage | $V_{OH}$ | $V_I$=$V_{IH}$ or $V_{IL}$ | $I_O$=-100uA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V | $V_{CCO}$-0.1 | - | - | V |
| | | | $I_O$=-3mA; $V_{CC(A)}$=$V_{CC(B)}$=1.1V | 0.85 | - | - | V |
| | | | $I_O$=-6mA; $V_{CC(A)}$=$V_{CC(B)}$=1.4V | 1.05 | - | - | V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | $I_O$=-8 mA; $V_{CC(A)}$=$V_{CC(B)}$=1.65V | 1.2 | - | - | V |
| | | | $I_O$=-9mA; $V_{CC(A)}$=$V_{CC(B)}$=2.3V | 1.75 | - | - | V |
| | | | $I_O$=-12mA; $V_{CC(A)}$=$V_{CC(B)}$=3.0V | 2.3 | - | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$=$V_{IH}$ or $V_{IL}$ | $I_O$=100uA; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V | - | - | 0.1 | V |
| | | | $I_O$=3mA; $V_{CC(A)}$=$V_{CC(B)}$=1.1V | - | - | 0.25 | V |
| | | | $I_O$=6mA; $V_{CC(A)}$=$V_{CC(B)}$=1.4V | - | - | 0.35 | V |
| | | | $I_O$=8mA; $V_{CC(A)}$=$V_{CC(B)}$=1.65V | - | - | 0.45 | V |
| | | | $I_O$=9mA; $V_{CC(A)}$=$V_{CC(B)}$=2.3V | - | - | 0.55 | V |
| | | | $I_O$=12mA; $V_{CC(A)}$=$V_{CC(B)}$=3.0V | - | - | 0.7 | V |
| input leakage current | $I_I$ | DIR input; $V_I$=0V or 3.6V; $V_{CC(A)}$=$V_{CC(B)}$=0.8V to 3.6V | | - | - | ±1.5 | uA |
| bus hold LOW current | $I_{BHL}$ | A or B port[3] | $V_I$=0.49V; $V_{CC(A)}$=$V_{CC(B)}$=1.4V | 15 | - | - | uA |
| | | | $V_I$=0.58V; $V_{CC(A)}$=$V_{CC(B)}$=1.65V | 25 | - | - | uA |
| | | | $V_I$=0.70V; $V_{CC(A)}$=$V_{CC(B)}$=2.3V | 45 | - | - | uA |
| | | | $V_I$=0.80V; $V_{CC(A)}$=$V_{CC(B)}$=3.0V | 90 | - | - | uA |
| bus hold HIGH current | $I_{BHH}$ | A or B port[4] | $V_I$=0.91V; $V_{CC(A)}$=$V_{CC(B)}$=1.4V | -15 | - | - | uA |
| | | | $V_I$=1.07V; $V_{CC(A)}$=$V_{CC(B)}$=1.65V | -25 | - | - | uA |
| | | | $V_I$=1.60V; $V_{CC(A)}$=$V_{CC(B)}$=2.3V | -45 | - | - | uA |
| | | | $V_I$=2.00V; $V_{CC(A)}$=$V_{CC(B)}$=3.0V | -100 | - | - | uA |
| bus hold LOW overdrive current | $I_{BHLO}$ | A or B port[5] | $V_{CC(A)}$=$V_{CC(B)}$=1.6V | 125 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=1.95V | 200 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=2.7V | 300 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=3.6V | 500 | - | - | uA |
| bus hold HIGH overdrive current | $I_{BHHO}$ | A or B port[6] | $V_{CC(A)}$=$V_{CC(B)}$=1.6V | -125 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=1.95V | -200 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=2.7V | -300 | - | - | uA |
| | | | $V_{CC(A)}$=$V_{CC(B)}$=3.6V | -500 | - | - | uA |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| OFF-state output current | $I_{OZ}$ | A or B port; $V_O$=0V or $V_{CCO}$; $V_{CC(A)}$=$V_{CC(B)}$=0.8 to 3.6V[7] | | - | - | ±7.5 | uA |
| power-off leakage current | $I_{OFF}$ | A port; $V_I$ or $V_O$=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0.8V to 3.6V | | - | - | ±35 | uA |
| | | B port; $V_I$ or $V_O$=0V to 3.6V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0.8V to 3.6V | | - | - | ±35 | uA |
| supply current | $I_{CC}$ | A port; $V_I$=0V or $V_{CCI}$; $I_O$=0A | $V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V | - | - | 11.5 | uA |
| | | | $V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V | - | - | 11.5 | uA |
| | | | $V_{CC(A)}$=0V; $V_{CC(B)}$=3.6V | -8 | - | - | uA |
| | | B port; $V_I$=0V or $V_{CCI}$; $I_O$=0A | $V_{CC(A)}$=0.8V to 3.6V; $V_{CC(B)}$=0.8V to 3.6V | - | - | 11.5 | uA |
| | | | $V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V | -8 | - | - | uA |
| | | | $V_{CC(A)}$=0V; $V_{CC(B)}$=3.6V | - | - | 11.5 | uA |
| | | A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); $I_O$=0A;$V_I$=0V or $V_{CCI}$; $V_{CC(A)}$=0.8V to 3.6V;$V_{CC(B)}$=0.8V to 3.6V | | - | - | 23 | uA |

Note:

[1] $V_{CCO}$ is the supply voltage associated with the output port.

[2] $V_{CCI}$ is the supply voltage associated with the data input port.

[3] The bus hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max. $I_{BHL}$ should be measured after lowering $V_I$ to GND and then raising it to $V_{IL}$ max.

[4] The bus hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min. $I_{BHH}$ should be measured after raising $V_I$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.

[5] An external driver must source at least $I_{BHLO}$ to switch this node from LOW to HIGH.

[6] An external driver must sink at least $I_{BHHO}$ to switch this node from HIGH to LOW.

[7] For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

### 3.3.4、AC Characteristics 1

($T_{amb}$=25℃, $V_{CC(A)}$=0.8V, voltages are referenced to GND (ground=0V), unless otherwise specified)[1][2]

| Parameter | Symbol | Conditions | $V_{CC(B)}$ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 0.8V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| propagation delay | $t_{pd}$ | A to B | 15.8 | 8.4 | 8.0 | 8.0 | 8.7 | 9.5 | ns |
| | | B to A | 15.8 | 12.7 | 12.4 | 12.2 | 12.0 | 11.8 | ns |
| disable time | $t_{dis}$ | DIR to A | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | ns |
| | | DIR to B | 11.7 | 7.9 | 7.6 | 8.2 | 8.7 | 10.2 | ns |
| enable time | $t_{en}$ | DIR to A | 27.5 | 20.6 | 20.0 | 20.4 | 20.7 | 22.0 | ns |
| | | DIR to B | 28.0 | 20.6 | 20.2 | 20.2 | 20.9 | 21.7 | ns |

Note:

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.

[2] $t_{en}$ is a calculated value using the formula shown in Section 5.4

### 3.3.5、AC Characteristics 2

($T_{amb}$=25℃, $V_{CC(B)}$=0.8V, voltages are referenced to GND (ground=0V), unless otherwise specified)[1][2]

| Parameter | Symbol | Conditions | $V_{CC(A)}$ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 0.8V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| propagation delay | $t_{pd}$ | A to B | 15.8 | 12.7 | 12.4 | 12.2 | 12.0 | 11.8 | ns |
| | | B to A | 15.8 | 8.4 | 8.0 | 8.0 | 8.7 | 9.5 | ns |
| disable time | $t_{dis}$ | DIR to A | 12.2 | 4.9 | 3.8 | 3.7 | 2.8 | 3.4 | ns |
| | | DIR to B | 11.7 | 9.2 | 9.0 | 8.8 | 8.7 | 8.6 | ns |
| enable time | $t_{en}$ | DIR to A | 27.5 | 17.6 | 17.0 | 16.8 | 17.4 | 18.1 | ns |
| | | DIR to B | 28.0 | 17.6 | 16.2 | 15.9 | 14.8 | 15.2 | ns |

Note:

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.

[2] $t_{en}$ is a calculated value using the formula shown in Section 5.4

### 3.3.6、AC Characteristics 3

($T_{amb}$=25℃, $V_{CC(A)}$=$V_{CC(B)}$=0.8V, voltages are referenced to GND (ground=0V), unless otherwise specified)[1][2]

| Parameter | Symbol | Conditions | $V_{CC(A)}$ and $V_{CC(B)}$ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 0.8V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| power dissipation capacitance | $C_{PD}$ | A port: (direction A to B); B port: (direction B to A) | 1 | 2 | 2 | 2 | 2 | 2 | pF |
| | | A port: (direction B to A); B port: (direction A to B) | 9 | 11 | 11 | 12 | 14 | 17 | pF |

Note:

[1] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\Sigma(C_L\times V_{CC}^2\times f_o)$ where:

$f_i$=input frequency in MHz;

$f_o$=output frequency in MHz;

$C_L$=load capacitance in pF;

$V_{CC}$=supply voltage in V;

N=number of inputs switching;

$\Sigma(C_L\times V_{CC}^2\times f_o)$ = sum of the outputs.

[2] $f_i$=10MHz; $V_I$=GND to $V_{CC}$; $t_r$=$t_f$=1ns; $C_L$=0pF; $R_L$=∞Ω.

### 3.3.7、AC Characteristics 4

($T_{amb}$=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified)[1][2]

| Parameter | Symbol | Conditions | $V_{CC(B)}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2V±0.1V | | 1.5V±0.1V | | 1.8V±0.15V | | 2.5V±0.2V | | 3.3V±0.3V | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **$V_{CC(A)}$=1.1V to 1.3V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 9.0 | 0.7 | 6.8 | 0.6 | 6.1 | 0.5 | 5.7 | 0.5 | 6.1 | ns |
| | | B to A | 1.0 | 9.0 | 0.8 | 8.0 | 0.7 | 7.7 | 0.6 | 7.2 | 0.5 | 7.1 | ns |
| disable time | $t_{dis}$ | DIR to A | 2.2 | 8.8 | 2.2 | 8.8 | 2.2 | 8.8 | 2.2 | 8.8 | 2.2 | 8.8 | ns |
| | | DIR to B | 2.2 | 8.4 | 1.8 | 6.7 | 2.0 | 6.9 | 1.7 | 6.2 | 2.4 | 7.2 | ns |
| enable time | $t_{en}$ | DIR to A | - | 17.4 | - | 14.7 | - | 14.6 | - | 13.4 | - | 14.3 | ns |
| | | DIR to B | - | 17.8 | - | 15.6 | - | 14.9 | - | 14.5 | - | 14.9 | ns |
| **$V_{CC(A)}$=1.4V to 1.6V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 8.0 | 0.7 | 5.4 | 0.6 | 4.6 | 0.5 | 3.7 | 0.5 | 3.5 | ns |
| | | B to A | 1.0 | 6.8 | 0.8 | 5.4 | 0.7 | 5.1 | 0.6 | 4.7 | 0.5 | 4.5 | ns |
| disable time | $t_{dis}$ | DIR to A | 1.6 | 6.3 | 1.6 | 6.3 | 1.6 | 6.3 | 1.6 | 6.3 | 1.6 | 6.3 | ns |
| | | DIR to B | 2.0 | 7.6 | 1.8 | 5.9 | 1.6 | 6.0 | 1.2 | 4.8 | 1.7 | 5.5 | ns |
| enable time | $t_{en}$ | DIR to A | - | 14.4 | - | 11.3 | - | 11.1 | - | 9.5 | - | 10.0 | ns |
| | | DIR to B | - | 14.3 | - | 11.7 | - | 10.9 | - | 10.0 | - | 9.8 | ns |
| **$V_{CC(A)}$=1.65V to 1.95V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 7.7 | 0.6 | 5.1 | 0.5 | 4.3 | 0.5 | 3.4 | 0.5 | 3.1 | ns |
| | | B to A | 1.0 | 6.1 | 0.7 | 4.6 | 0.5 | 4.4 | 0.5 | 3.9 | 0.5 | 3.7 | ns |
| disable time | $t_{dis}$ | DIR to A | 1.6 | 5.5 | 1.6 | 5.5 | 1.6 | 5.5 | 1.6 | 5.5 | 1.6 | 5.5 | ns |
| | | DIR to B | 1.8 | 7.8 | 1.8 | 5.7 | 1.4 | 5.8 | 1.0 | 4.5 | 1.5 | 5.2 | ns |
| enable time | $t_{en}$ | DIR to A | - | 13.9 | - | 10.3 | - | 10.2 | - | 8.4 | - | 8.9 | ns |
| | | DIR to B | - | 13.2 | - | 10.6 | - | 9.8 | - | 8.9 | - | 8.6 | ns |
| **$V_{CC(A)}$=2.3V to 2.7V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 7.2 | 0.5 | 4.7 | 0.5 | 3.9 | 0.5 | 3.0 | 0.5 | 2.6 | ns |
| | | B to A | 1.0 | 5.7 | 0.6 | 3.8 | 0.5 | 3.4 | 0.5 | 3.0 | 0.5 | 2.8 | ns |
| disable time | $t_{dis}$ | DIR to A | 1.5 | 4.2 | 1.5 | 4.2 | 1.5 | 4.2 | 1.5 | 4.2 | 1.5 | 4.2 | ns |
| | | DIR to B | 1.7 | 7.3 | 2.0 | 5.2 | 1.5 | 5.1 | 0.6 | 4.2 | 1.1 | 4.8 | ns |
| enable time | $t_{en}$ | DIR to A | - | 13.0 | - | 9.0 | - | 8.5 | - | 7.2 | - | 7.6 | ns |
| | | DIR to B | - | 11.4 | - | 8.9 | - | 8.1 | - | 7.2 | - | 6.8 | ns |
| **$V_{CC(A)}$=3.0V to 3.6V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 7.1 | 0.5 | 4.5 | 0.5 | 3.7 | 0.5 | 2.8 | 0.5 | 2.4 | ns |
| | | B to A | 1.0 | 6.1 | 0.6 | 3.6 | 0.5 | 3.1 | 0.5 | 2.6 | 0.5 | 2.4 | ns |
| disable time | $t_{dis}$ | DIR to A | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | ns |
| | | DIR to B | 1.7 | 7.2 | 0.7 | 5.5 | 0.6 | 5.5 | 0.7 | 4.1 | 1.7 | 4.7 | ns |
| enable time | $t_{en}$ | DIR to A | - | 13.3 | - | 9.1 | - | 8.6 | - | 6.7 | - | 7.1 | ns |
| | | DIR to B | - | 11.8 | - | 9.2 | - | 8.4 | - | 7.5 | - | 7.1 | ns |

Note:

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.

[2] $t_{en}$ is a calculated value using the formula shown in Section 5.4

### 3.3.8、AC Characteristics 5

($T_{amb}$=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified)[1][2]

| Parameter | Symbol | Conditions | $V_{CC(B)}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2V±0.1V | | 1.5V±0.1V | | 1.8V±0.15V | | 2.5V±0.2V | | 3.3V±0.3V | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **$V_{CC(A)}$=1.1V to 1.3V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 9.9 | 0.7 | 7.5 | 0.6 | 6.8 | 0.5 | 6.3 | 0.5 | 6.8 | ns |
| | | B to A | 1.0 | 9.9 | 0.8 | 8.8 | 0.7 | 8.5 | 0.6 | 8.0 | 0.5 | 7.9 | ns |
| disable time | $t_{dis}$ | DIR to A | 2.2 | 9.7 | 2.2 | 9.7 | 2.2 | 9.7 | 2.2 | 9.7 | 2.2 | 9.7 | ns |
| | | DIR to B | 2.2 | 9.2 | 1.8 | 7.4 | 2.0 | 7.6 | 1.7 | 6.9 | 2.4 | 8.0 | ns |
| enable time | $t_{en}$ | DIR to A | - | 19.1 | - | 16.2 | - | 16.1 | - | 14.9 | - | 15.9 | ns |
| | | DIR to B | - | 19.6 | - | 17.2 | - | 16.5 | - | 16.0 | - | 16.5 | ns |
| **$V_{CC(A)}$=1.4V to 1.6V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 8.8 | 0.7 | 6.0 | 0.6 | 5.1 | 0.5 | 4.1 | 0.5 | 3.9 | ns |
| | | B to A | 1.0 | 7.5 | 0.8 | 6.0 | 0.7 | 5.7 | 0.6 | 5.2 | 0.5 | 5.0 | ns |
| disable time | $t_{dis}$ | DIR to A | 1.6 | 7.0 | 1.6 | 7.0 | 1.6 | 7.0 | 1.6 | 7.0 | 1.6 | 7.0 | ns |
| | | DIR to B | 2.0 | 8.3 | 1.8 | 6.5 | 1.6 | 6.6 | 1.2 | 5.3 | 1.7 | 6.1 | ns |
| enable time | $t_{en}$ | DIR to A | - | 15.8 | - | 12.5 | - | 12.3 | - | 10.5 | - | 11.1 | ns |
| | | DIR to B | - | 15.8 | - | 13.0 | - | 12.7 | - | 11.1 | - | 10.9 | ns |
| **$V_{CC(A)}$=1.65V to 1.95V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 8.5 | 0.6 | 5.7 | 0.5 | 4.8 | 0.5 | 3.8 | 0.5 | 3.5 | ns |
| | | B to A | 1.0 | 6.8 | 0.7 | 5.1 | 0.5 | 4.9 | 0.5 | 4.3 | 0.5 | 4.1 | ns |
| disable time | $t_{dis}$ | DIR to A | 1.6 | 6.1 | 1.6 | 6.1 | 1.6 | 6.1 | 1.6 | 6.1 | 1.6 | 6.1 | ns |
| | | DIR to B | 1.8 | 8.6 | 1.8 | 6.3 | 1.4 | 6.4 | 1.0 | 5.0 | 1.5 | 5.8 | ns |
| enable time | $t_{en}$ | DIR to A | - | 15.4 | - | 11.4 | - | 11.3 | - | 9.3 | - | 9.9 | ns |
| | | DIR to B | - | 14.6 | - | 11.8 | - | 10.9 | - | 9.9 | - | 9.6 | ns |
| **$V_{CC(A)}$=2.3V to 2.7V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 8.2 | 0.5 | 5.2 | 0.5 | 4.3 | 0.5 | 3.3 | 0.5 | 2.9 | ns |
| | | B to A | 1.0 | 6.3 | 0.6 | 4.2 | 0.5 | 3.8 | 0.5 | 3.3 | 0.5 | 3.1 | ns |
| disable time | $t_{dis}$ | DIR to A | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | 1.5 | 4.7 | ns |
| | | DIR to B | 1.7 | 8.0 | 2.0 | 5.8 | 1.5 | 5.7 | 0.6 | 4.7 | 1.1 | 5.3 | ns |
| enable time | $t_{en}$ | DIR to A | - | 14.3 | - | 10.0 | - | 9.5 | - | 8.0 | - | 8.4 | ns |
| | | DIR to B | - | 12.7 | - | 9.9 | - | 9.0 | - | 8.0 | - | 7.6 | ns |
| **$V_{CC(A)}$=3.0V to 3.6V** | | | | | | | | | | | | | |
| propagation delay | $t_{pd}$ | A to B | 1.0 | 7.9 | 0.5 | 5.0 | 0.5 | 4.1 | 0.5 | 3.1 | 0.5 | 2.7 | ns |
| | | B to A | 1.0 | 6.8 | 0.6 | 4.0 | 0.5 | 3.5 | 0.5 | 2.9 | 0.5 | 2.7 | ns |
| disable time | $t_{dis}$ | DIR to A | 1.5 | 5.2 | 1.5 | 5.2 | 1.5 | 5.2 | 1.5 | 5.2 | 1.5 | 5.2 | ns |
| | | DIR to B | 1.7 | 7.9 | 0.7 | 6.1 | 0.6 | 6.1 | 0.7 | 4.6 | 1.7 | 5.2 | ns |
| enable time | $t_{en}$ | DIR to A | - | 14.7 | - | 10.1 | - | 9.6 | - | 7.5 | - | 7.9 | ns |
| | | DIR to B | - | 13.1 | - | 10.2 | - | 9.3 | - | 8.3 | - | 7.9 | ns |

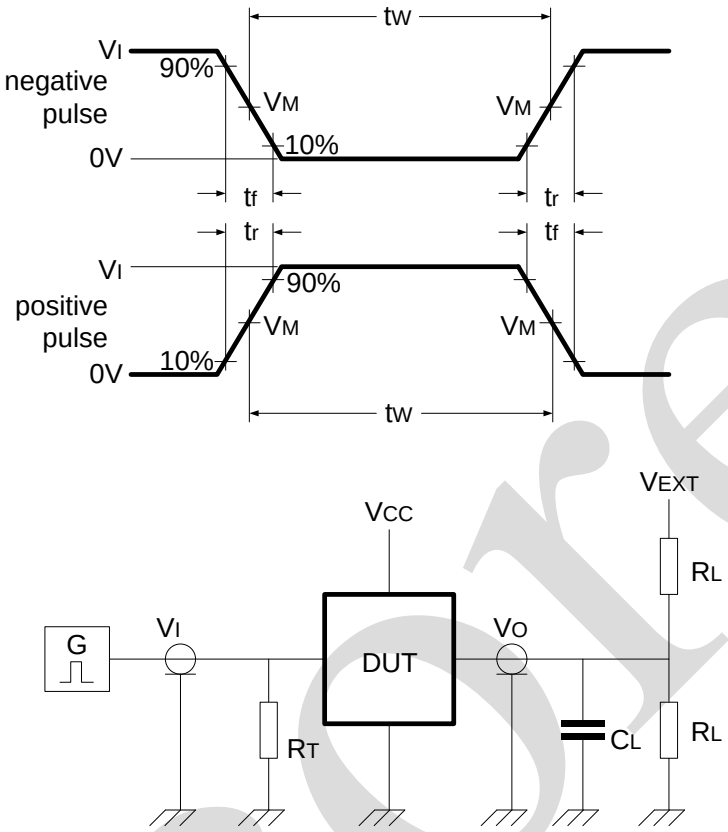
Note:

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$; $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.

[2] $t_{en}$ is a calculated value using the formula shown in Section 5.4

## 4、Testing Circuit

### 4.1、AC Testing Circuit




$R_L$=Load resistance.

$C_L$=Load capacitance including jig and probe capacitance.

$R_T$=Termination resistance.

$V_{EXT}$=External voltage for measuring switching times.

Figure 3. Test circuit for measuring switching times

### 4.2、Test Data

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC(A)}$, $V_{CC(B)}$ | $V_I$[1] | $\Delta t/\Delta V$[2] | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$[3] |
| 1.1V to 1.6V | $V_{CCI}$ | ≤1.0ns/V | 15pF | 2kΩ | open | GND | $2V_{CCO}$ |
| 1.65V to 2.7V | $V_{CCI}$ | ≤1.0ns/V | 15pF | 2kΩ | open | GND | $2V_{CCO}$ |
| 3.0V to 3.6V | $V_{CCI}$ | ≤1.0ns/V | 15pF | 2kΩ | open | GND | $2V_{CCO}$ |

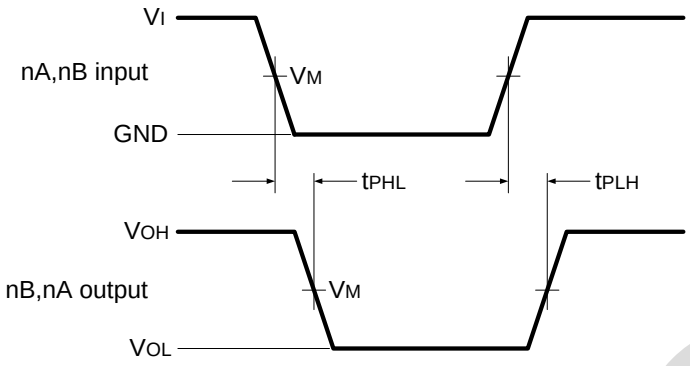
Note:

[1] $V_{CCI}$ is the supply voltage associated with the data input port.

[2] dV/dt≥1.0V/ns

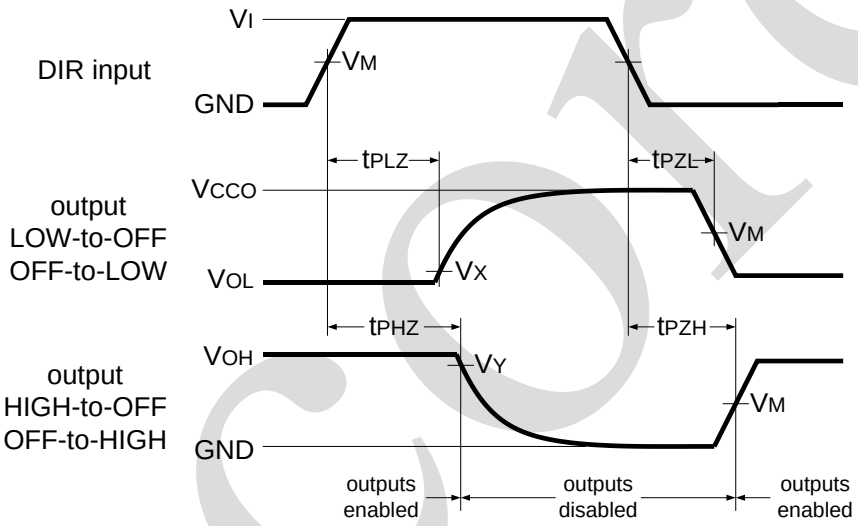
[3] $V_{CCO}$ is the supply voltage associated with the output port.

### 4.3、AC Testing Waveforms




$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Figure 4. The data input (nA, nB) to output (nB, nA) propagation delay times




$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Figure 5. 3-state enable and disable times

### 4.4、Measurement points

| **Supply voltage** | **Input[1]** | **Output[2]** | | |
|---|---|---|---|---|
| **$V_{CC(A)}$, $V_{CC(B)}$** | **$V_M$** | **$V_M$** | **$V_X$** | **$V_Y$** |
| 1.1V to 1.6V | $0.5V_{CCI}$ | $0.5V_{CCO}$ | $V_{OL}$+0.1V | $V_{OH}$-0.1V |
| 1.65V to 2.7V | $0.5V_{CCI}$ | $0.5V_{CCO}$ | $V_{OL}$+0.15V | $V_{OH}$-0.15V |
| 3.0V to 3.6V | $0.5V_{CCI}$ | $0.5V_{CCO}$ | $V_{OL}$+0.3V | $V_{OH}$-0.3V |

Note:

[1] $V_{CCI}$ is the supply voltage associated with the data input port.

[2] $V_{CCO}$ is the supply voltage associated with the output port.

## 5、Typical Application Circuit And Application Note

### 5.1、Unidirectional logic level-shifting application

The circuit given in Figure 6 is an example of the AiP74AVCH2T45 being used in an unidirectional logic level-shifting application.

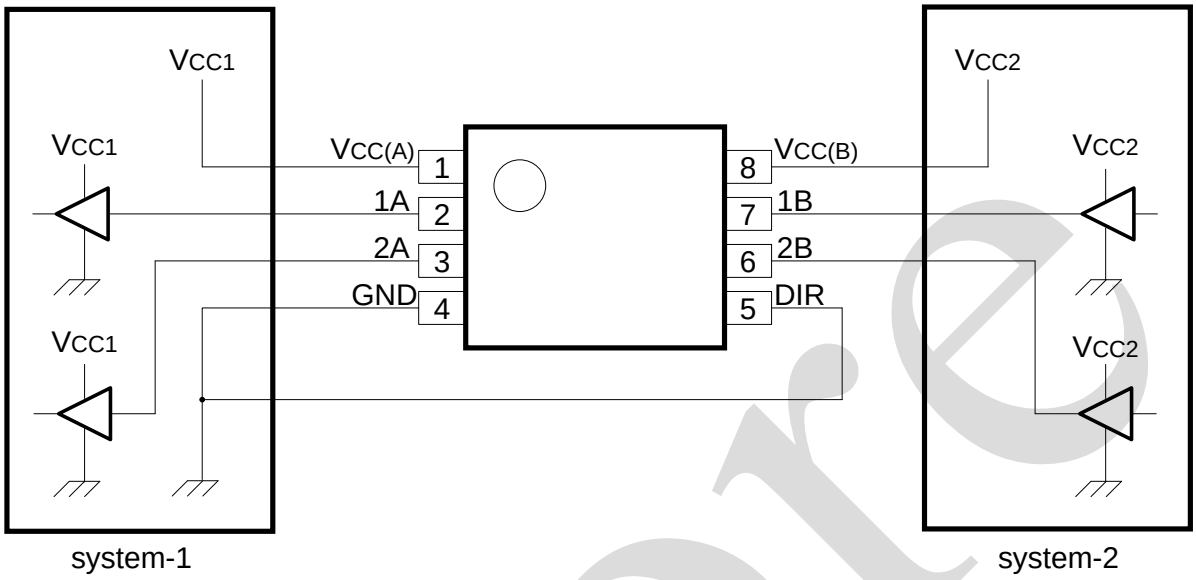



Figure 6. Unidirectional logic level-shifting application

**Unidirectional logic level-shifting application**

| Pin | Name | Function | Description |
|---|---|---|---|
| 1 | $V_{CC(A)}$ | $V_{CC1}$ | supply voltage of system-1 (0.8V to 3.6V) |
| 2 | 1A | OUT1 | output level depends on $V_{CC1}$ voltage |
| 3 | 2A | OUT2 | output level depends on $V_{CC1}$ voltage |
| 4 | GND | GND | device GND |
| 5 | DIR | DIR | the GND (LOW level) determines B port to A port direction |
| 6 | 2B | IN2 | input threshold value depends on $V_{CC2}$ voltage |
| 7 | 1B | IN1 | input threshold value depends on $V_{CC2}$ voltage |
| 8 | $V_{CC(B)}$ | $V_{CC2}$ | supply voltage of system-2 (0.8V to 3.6V) |

### 5.2、Bidirectional logic level-shifting application

Figure 7 shows the AiP74AVCH2T45 being used in a bidirectional logic level-shifting application. Since the device does not have an output enable (OE) pin, the system designer should take precautions to avoid bus contention between system-1 and system-2 when changing directions.

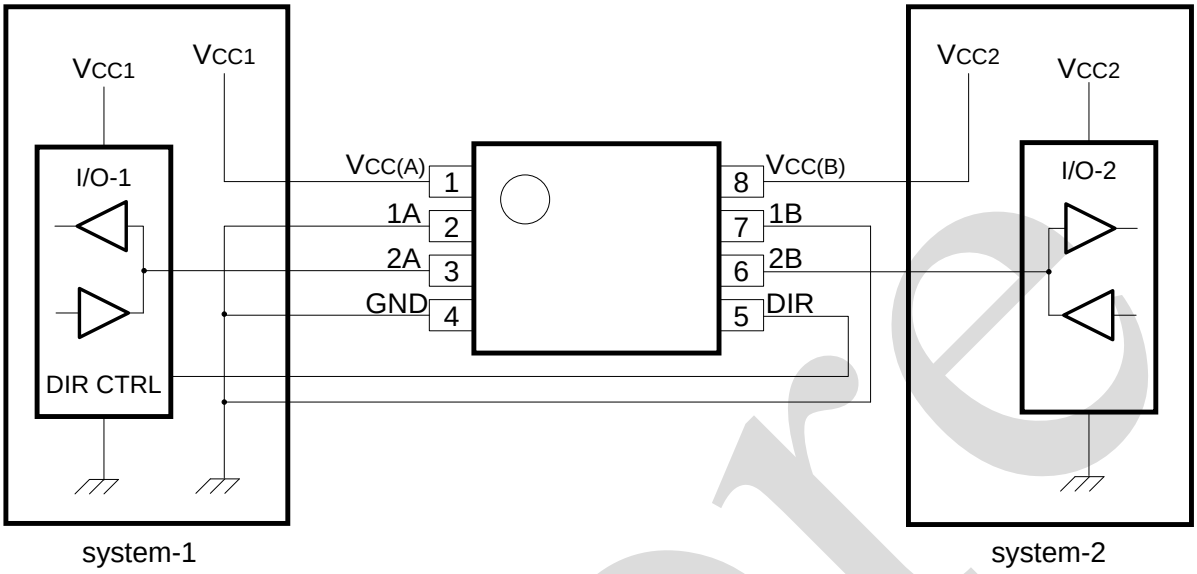



Figure 7. Bidirectional logic level-shifting application

Table 1 gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

**Table 1. Bidirectional logic level-shifting application[1]**

| State | DIR CTRL | I/O-1 | I/O-2 | Description |
|---|---|---|---|---|
| 1 | H | output | input | system-1 data to system-2 |
| 2 | H | Z | Z | system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold. |
| 3 | L | Z | Z | DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold. |
| 4 | L | input | output | system-2 data to system-1 |

Note:

[1] H=HIGH voltage level;
L=LOW voltage level;
Z=high-impedance OFF-state.

### 5.3、Power-up considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

**Table 2. Typicaltotal supply current ($I_{CC(A)}$ + $I_{CC(B)}$)**

| $V_{CC(A)}$ | $V_{CC(B)}$ | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 0V | 0.8V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| 0V | 0 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | uA |
| 0.8V | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.7 | 2.3 | uA |
| 1.2V | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.3 | 1.4 | uA |
| 1.5V | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.9 | uA |
| 1.8V | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.5 | uA |
| 2.5V | 0.1 | 0.7 | 0.3 | 0.1 | 0.1 | 0.1 | 0.1 | uA |
| 3.3V | 0.1 | 2.3 | 1.4 | 0.9 | 0.5 | 0.1 | 0.1 | uA |

### 5.4、Enable times

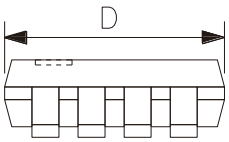
The enable times for the AiP74AVCH2T45 are calculated from the following formulas:

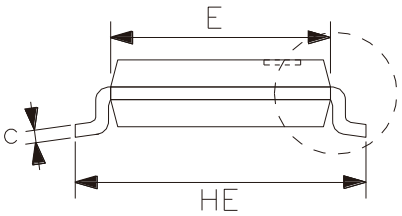
- $t_{en}$ (DIR to nA) = $t_{dis}$ (DIR to nB) + $t_{pd}$ (nB to nA)
- $t_{en}$ (DIR to nB) = $t_{dis}$ (DIR to nA) + $t_{pd}$ (nA to nB)

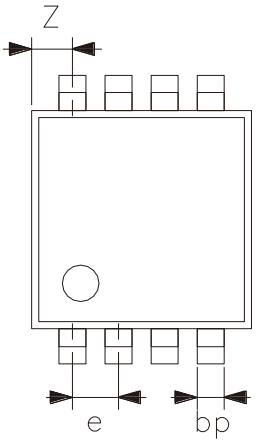
In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the AiP74AVCH2T45 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

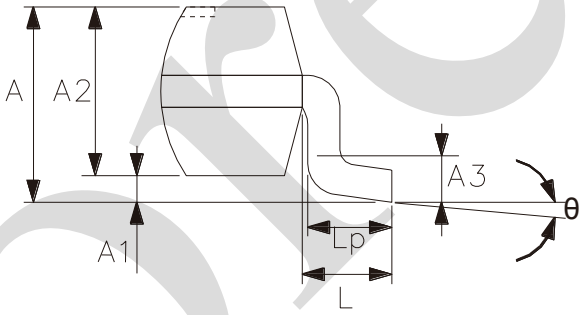
## 6、Package Information

### 6.1、TSSOP8



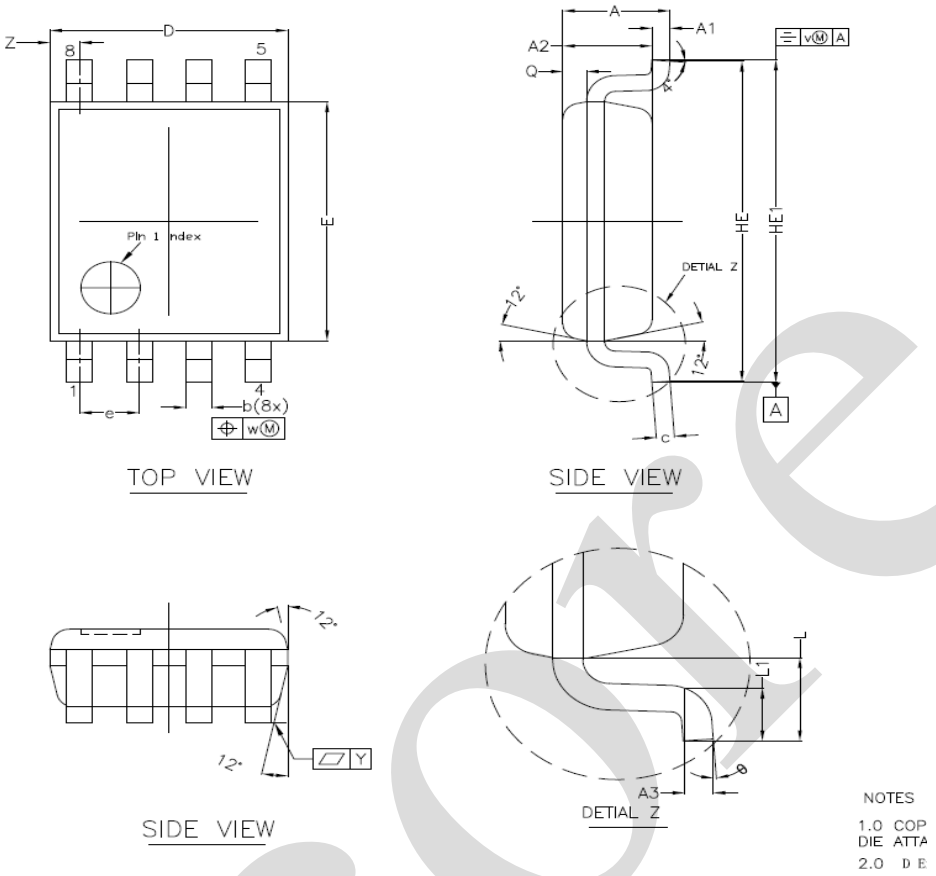




| Symbol | Dimensions (mm) | |
|---|---|---|
| | Min. | Max. |
| A | - | 1.10 |
| A1 | 0 | 0.15 |
| A2 | 0.75 | 0.95 |
| A3 | 0.25 | |
| bp | 0.22 | 0.38 |
| c | 0.08 | 0.18 |
| D | 2.90 | 3.10 |
| E | 2.90 | 3.10 |
| HE | 3.90 | 4.10 |
| L | 0.50 | |
| Lp | 0.33 | 0.47 |
| e | 0.65 | |
| Z | 0.35 | 0.70 |
| θ | 0 ° | 8 ° |

**6.2、VSSOP8**




| Symbol | Dimensions (mm) | |
|---|---|---|
| | Min. | Max. |
| A | - | 1.00 |
| A1 | 0.00 | 0.15 |
| A2 | 0.60 | 0.85 |
| A3 | 0.12 | |
| Q | 0.19 | 0.21 |
| b | 0.17 | 0.27 |
| c | 0.08 | 0.23 |
| D | 1.90 | 2.10 |
| E | 2.20 | 2.40 |
| HE | 3.00 | 3.20 |
| HE1 | 3.00 | 3.40 |
| e | 0.50 | |
| L | 0.40 | |
| L1 | 0.15 | 0.40 |
| Y | 0.10 | |
| Z | 0.10 | 0.40 |
| θ | 0 ° | 8 ° |

## 7、Statements And Notes

### 7.1、The name and content of Hazardous substances or Elements in the product

| Part name | Hazardous substances or Elements | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Lead and lead compounds | Mercury and mercury compounds | Cadmium and cadmium compounds | Hexavalent chromium compounds | Polybrominated biphenyls | Polybrominated biphenyl ethers | Dibutyl phthalate | Butylbenzyl phthalate | Di-2-ethylhexyl phthalate | Diisobutyl phthalate |
| Lead frame | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Plastic resin | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Chip | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| The lead | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Plastic sheet installed | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| explanation | ○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard.<br>×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements. | | | | | | | | | |

### 7.2、Notes

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