AiPGTL2003
8-Bit Bidirectional Low Voltage Translator

Product Specification

Specification Revision History：

Version	Date	Description
2023-05-A1	2023-05	New
2023-11-A2	2023-11	Modify General Description

Contents

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1、General Description

AiPGTL2003 is a voltage level translator. The circuit supports bidirectional multi-voltage level translation in the range of 0.8V to 5V without direction control.

Features:

- 8-channel bidirectional multi-voltage level translation
- support bidirectional multi-voltage level translation in the range of 0.8V to 5V, can be directly used for GTL, GTL+, LVTTL, TTL or 5V CMOS level
- transmission direction automatically adapted without direction control
- low ON-resistance when the translation channel is ON-state
- no power supply requirement, no latch-up risk
- low power consumption
- ESD-HBM:4000V
- package form: TSSOP20

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiPGTL2003TA20.TB	TSSOP20	AiPGTL2003	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm

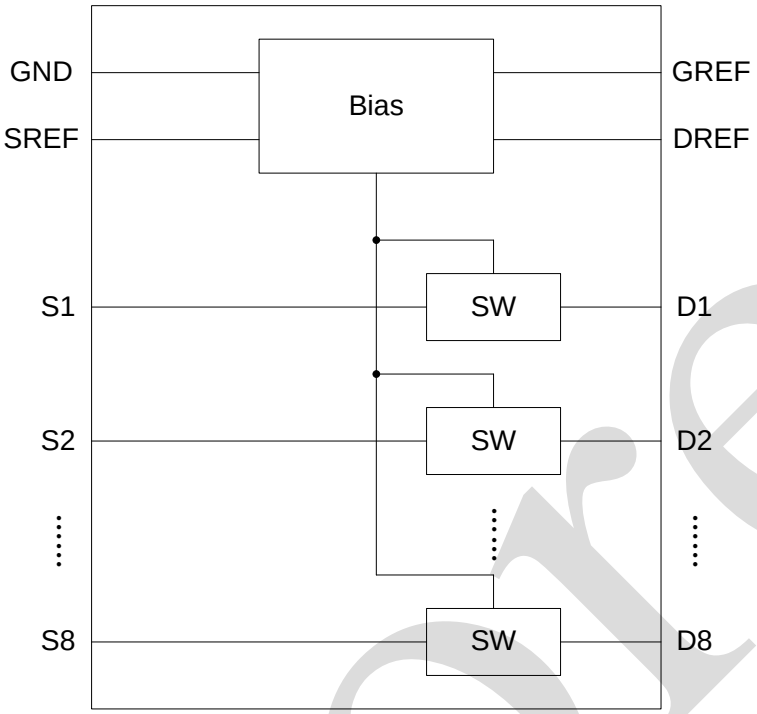
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiPGTL2003TA20.TR	TSSOP20	AiPGTL2003	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm

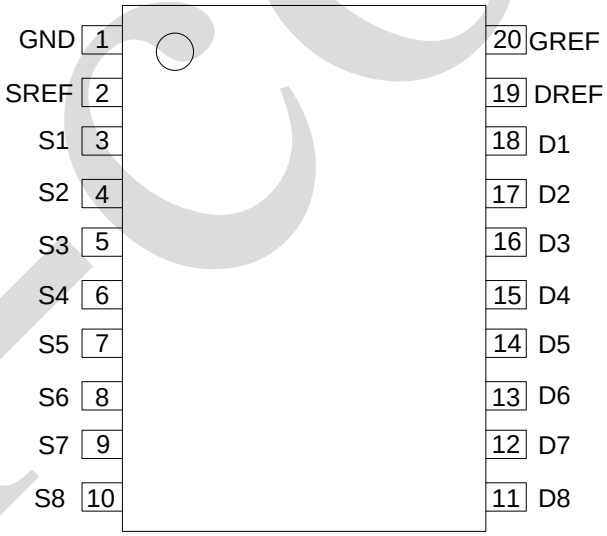
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Configurations



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2.3、Pin Description

Pin No.	Pin Name	I/O	Description
1	GND	Power	ground
2	SREF	I	S port reference voltage, connected to S port signal power supply
3 to 10	S1 to S8	IO	signal transmission port S
11 to 18	D8 to D1	IO	signal transmission port D
19	DREF	I	D port reference voltage, connected to D port signal power supply via 200K resistance
20	GREF	I	G port reference voltage, when connected to 0V, transmission channel is closed, and it is short circuited to DREF and connected to the D port signal power supply through a 200K resistance to achieve automatic adaptation of signal transmission direction

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, unless otherwise specified)

Characteristic	Symbol	Value	Unit
reference voltage 1	DREF	-0.3 to 7.0	V
reference voltage 2	SREF	-0.3 to 7.0	V
reference voltage 3	GREF	-0.3 to 7.0	V
input voltage	V_{IN}	-0.3 to 7.0	V
operating temperature	T_{amb}	-40 to 85	℃
storage temperature	T_{stg}	-65 to +150	℃
soldering temperature (10s)	T_L	260	℃

Note:

1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. These are only partial specified values and do not support functional operations for conditions other than those specified.
2) All voltage values are based on the ground port as the reference.

3.2、Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
DREF reference voltage	V_{DREF}	0	-	5.5	V
SREF reference voltage	V_{SREF}	0	-	5.5	V
GREF reference voltage	V_{GREF}	0	-	5.5	V
IO input voltage	V_{IN}	0	-	5.5	V
transmission channel current	I_{SW}	-	-	64	mA

3.3、Electrical Characteristics

(T_{amb}=-40 to 85℃, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LOW-level output voltage	V_{OL}	see Figure 1 VDD1=1.365V, VDD2=3V VDn=0.175V, VSn output or VSn=0.175V, VDn output Ipass=15.2mA	-	260	350	mV
input clamp voltage	Vclamp	Ii=-18mA, V_{GREF}=0V	-	-	-1.2	V
GREF input leakage current	I_{GREF}	V_{GREF}=0V	-	-	5	uA
ON resistance	Ron	VSn=0, I_O=64mA, V_{GREF}=4.5V	-	3.5	5	Ω
		VSn=0, I_O=64mA, V_{GREF}=3.0V	-	4.4	7	Ω
		VSn=0, I_O=64mA, V_{GREF}=2.3V	-	5.5	9	Ω
		VSn=0, I_O=64mA, V_{GREF}=1.5V	-	9	105	Ω
		VSn=0, I_O=30mA, V_{GREF}=1.5V	-	9	15	Ω
		VSn=2.4V, I_O=15mA, V_{GREF}=4.5V	-	7	10	Ω
		VSn=2.4V, I_O=15mA, V_{GREF}=3.0V	-	58	80	Ω
		VSn=1.7V, I_O=15mA, V_{GREF}=2.3V	-	50	70	Ω

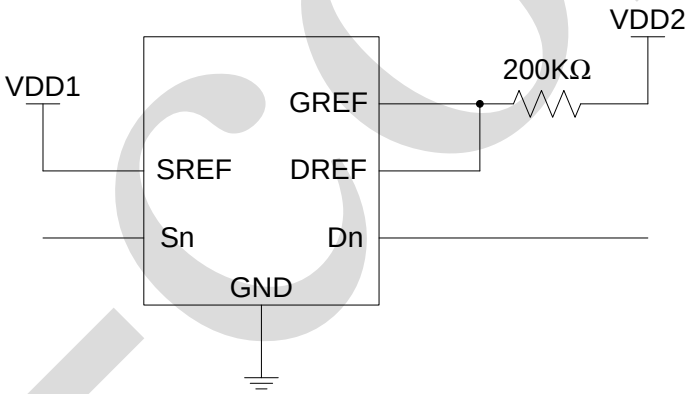


Figure 1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay 1 (see Figure 3)	t_{PLH} t_{PHL}	test circuit see Figure 2 VDD1=1.365V to 1.635V VDD2=3V to 3.6V VDD3=2.36V to 2.63V t_r=t_f≤3ns Sn input, Dn output	0.5	1.5	5.5	ns

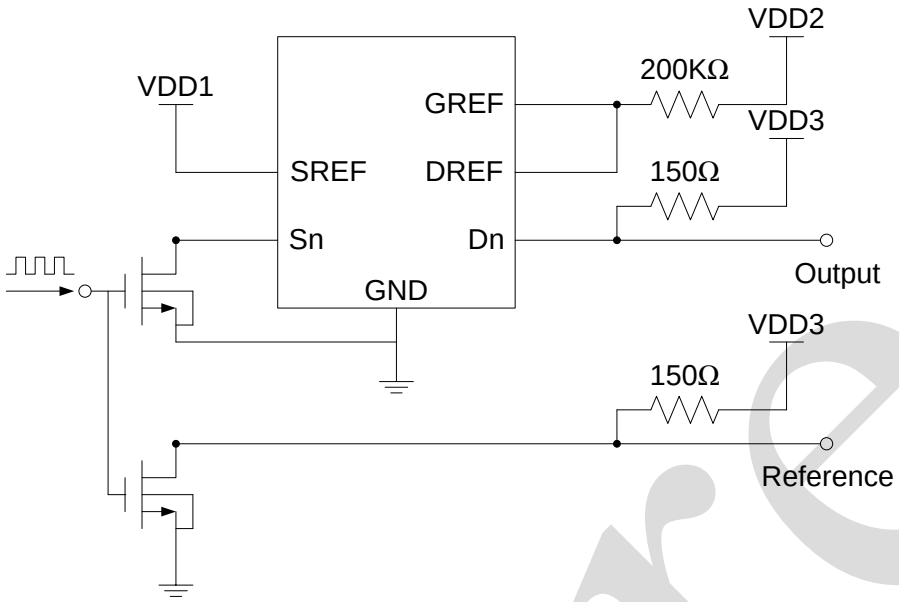


Figure 2

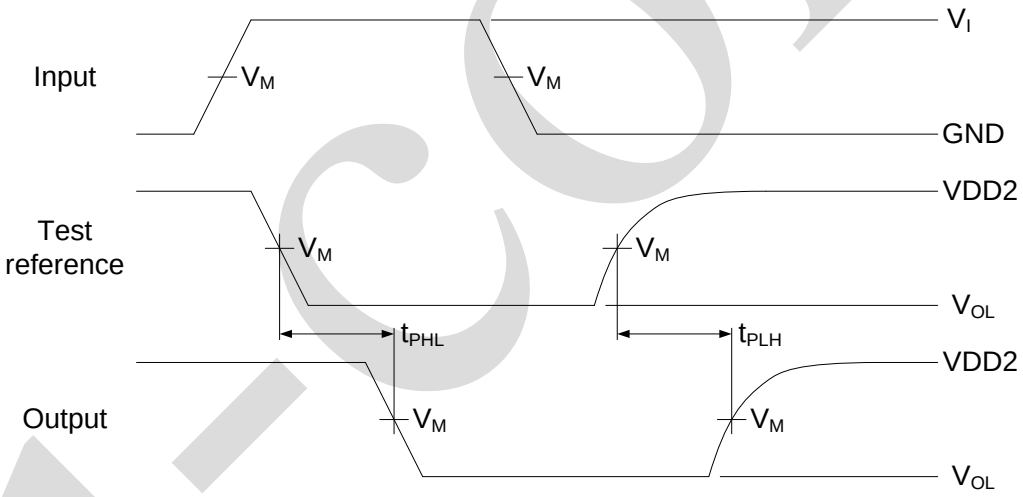


Figure 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay 2 (see Figure 5)	t_{pd}	test circuit see Figure 4 V_{GREF}=5V±0.5V DREF, SREF floating Sn input, Dn output or Dn input, Sn output	-	-	250	ps

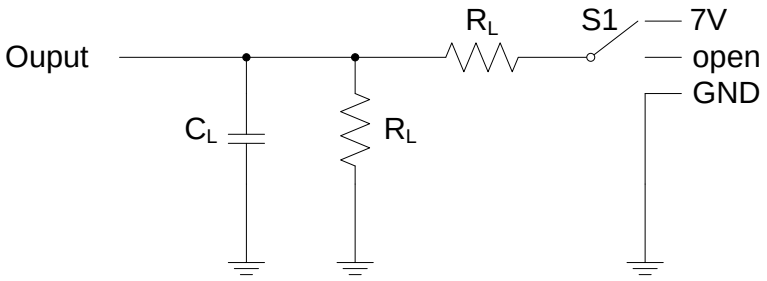


Figure 4

C_L=load capacitance including package, PCB and probe parasitic capacitance.

Test	C_L	R_L	S1
t_{pd}	50pF	500Ω	open

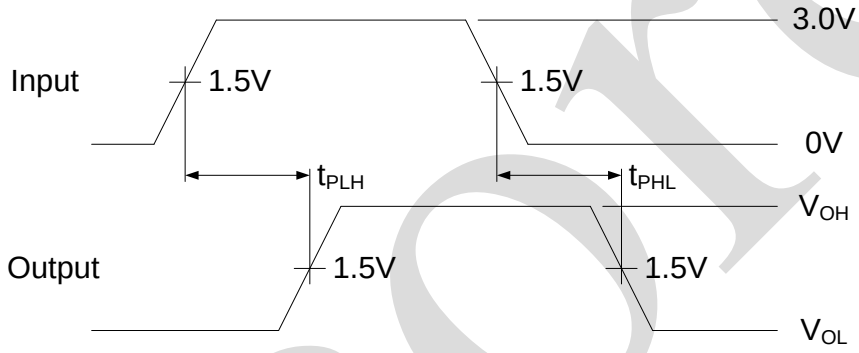


Figure 5

4、Function Description

4.1、Function Table

GREF	DREF	SREF	Dn input	Sn output	Transmission Channel
L	X	X	X	X	OFF
H(V_{GREF})	H(V_{DREF})	H(V_{SREF})	V_{DREF}	V_{SREF}	ON
H(V_{GREF})	H(V_{DREF})	H(V_{SREF})	L	L	ON

GREF	DREF	SREF	Sn input	Dn output	Transmission Channel
L	X	X	X	X	OFF
H(V_{GREF})	H(V_{DREF})	H(V_{SREF})	V_{SREF}	VH	ON
H(V_{GREF})	H(V_{DREF})	H(V_{SREF})	L	L	ON

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

V_{GREF}>V_{SREF} V_{DREF}>V_{SREF}, VH>V_{SREF} for normal operation

When V_{GREF} is 1.5V higher than V_{SREF}, the circuit has the best signal transmission performance.

When Sn is the output, Sn can be pulled up to V_{SREF} by external resistance or without external pull-up resistance.

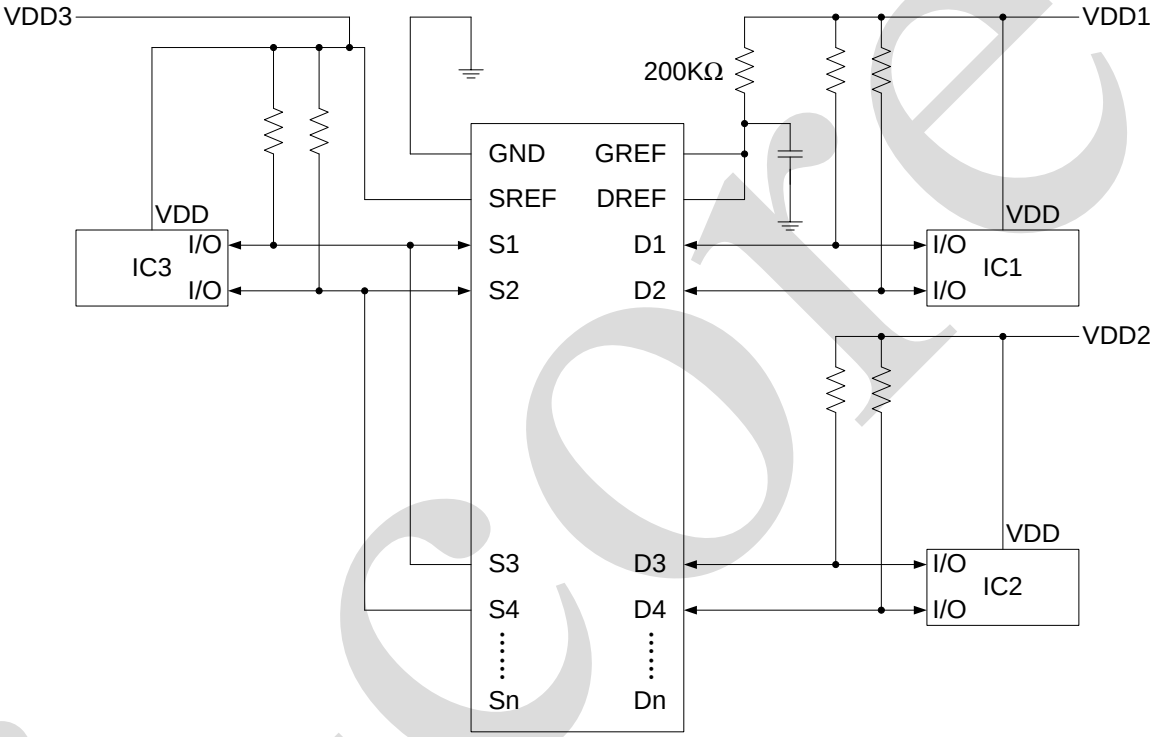
When Dn is the output, Dn must be pulled up through the external resistance to a higher level than V_{SREF}.

When Sn/Dn outputs LOW, LOW-level output voltage value is determined by LOW-level input voltage value, not by GND.

4.2、Bidirectional Translation Without Direction Control

When applied to bidirectional signal transmission, and there is no control signal to indicate the direction of signal transmission, the GREF must be connected to the DREF and connected to the higher level by a 200KΩ resistance, and a filter capacitor near the GREF port, while the SREF is connected to the lower level.

Both side signals can be push-pull or open-drain. But when signal is open-drain, an external pull-up resistance must be presented.



When VDD1≥VDD2≥VDD3, multi-power applications are allowed.

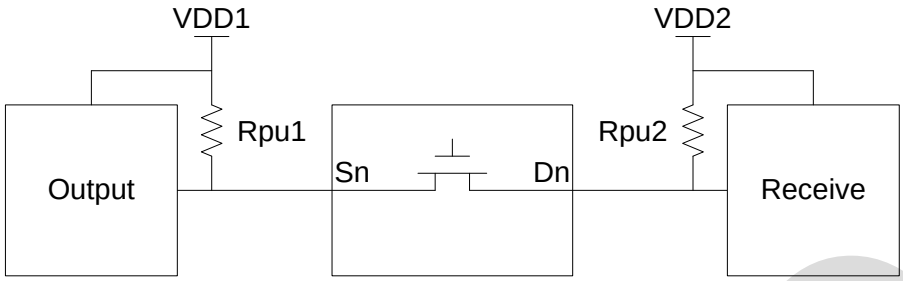
When VDD1≥VDD2≥VDD3+1.0V, the pull-up resistance of IO on the IC3 can be omitted.

4.3、Pull-up Resistor Sizing

Adding the pull-up resistance to IO can effectively improve the signal transmission efficiency and get a more complete waveform. Pull-up resistor value depends on several factors:

1. The low level driving ability of output device and the low level recognition ability of receive device
   When the output device outputs LOW-level, the current generated by the pull-up resistance of the Sn and Dn port will be absorbed by the low side drive of the output device, LOW-level of transmission will be pulled up. When the low level is pulled up beyond the low level recognition range of the receive device, the signal transmission will be abnormal. Therefore, the pull-up resistor should be selected according to the above factors, and the resistance value should not be set too small.
2. The rate of transmission signal
   When Sn is input, Dn is output, due to the requirement that VDD2 is higher than VDD1, this time due to the transmission principle of the circuit leads to the high level output of Dn port is to rely on Rpu2

pulled up, at this time the size of Rpu2 determines the rise rate of the signal of Dn, and further determines the highest frequency of the signal at Dn. Therefore, the resistance value cannot be set too large.

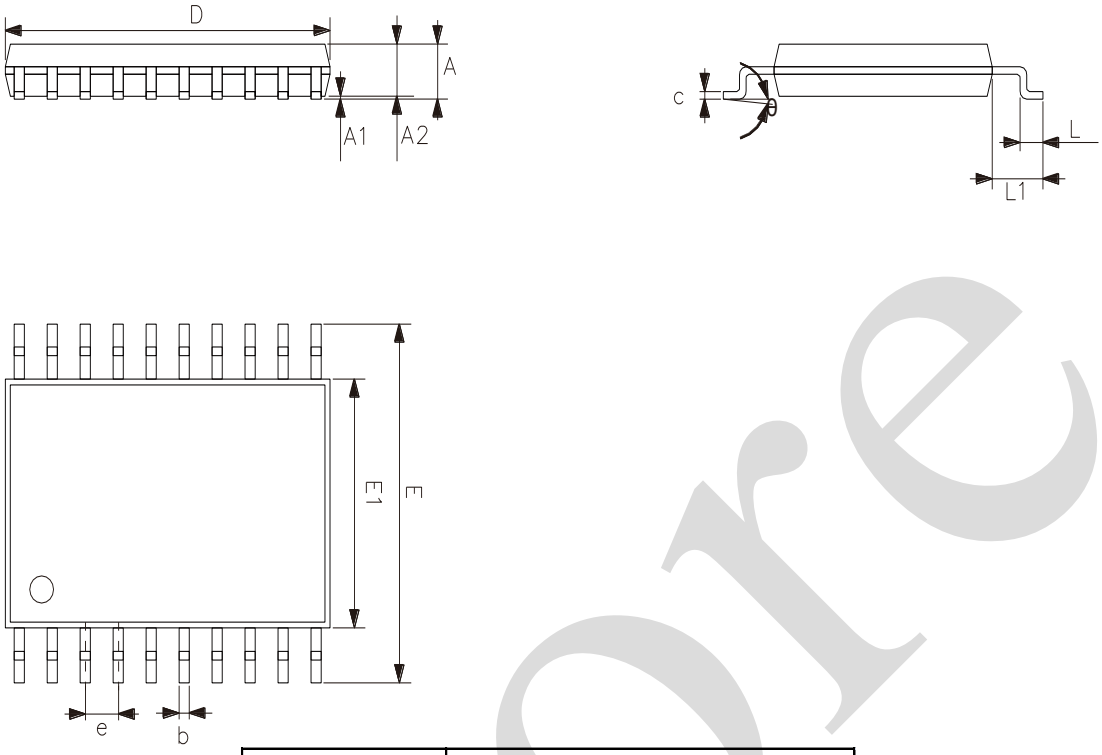


Pull-up resistor values:

LOW-level output current of output device V_{OL}=0.2V		**15mA**		**10mA**		**3mA**	
VDD1	**VDD2**	**Rpu1**	**Rpu2**	**Rpu1**	**Rpu2**	**Rpu1**	**Rpu2**
0.8	1.8	147	147	220	220	733	733
0.8	2.5	193	193	290	290	967	967
0.8	3.3	247	247	370	370	1233	1233
0.8	5.0	360	360	540	540	1800	1800
1.2	1.8	173	173	260	260	867	867
1.2	2.5	220	220	330	330	1100	1100
1.2	3.3	273	273	410	410	1367	1367
1.2	5.0	387	387	580	580	1933	1933
1.5	1.8	193	193	290	290	967	967
1.5	2.5	240	240	360	360	1200	1200
1.5	3.3	293	293	440	440	1467	1467
1.5	5.0	407	407	610	610	2033	2033
1.8	2.5	260	260	390	390	1300	1300
1.8	3.3	313	313	470	470	1567	1567
1.8	5.0	427	427	640	640	2133	2133
2.5	3.3	360	360	540	540	1800	1800
2.5	5.0	473	473	710	710	2367	2367
3.3	5.0	527	527	790	790	2633	2633
<VDD2	1.0	-	53	-	80	-	267
<VDD2	1.2	-	67	-	100	-	333
<VDD2	1.5	-	87	-	130	-	433
<VDD2	1.8	-	107	-	160	-	533
<VDD2	2.5	-	153	-	230	-	767
<VDD2	3.3	-	207	-	310	-	1033
<VDD2	5.0	-	320	-	480	-	1600

5、Package Information

5.1、TSSOP20



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

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6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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